

DEVICE SPECIFICATION

DRAFT

TDA935X/6X/8X series

TV signal processor-Teletext
decoder with embedded μ -Controller

Preliminary Device Specification

1999 Sep 28

Version: 1.3

Previous date: 1999 Aug 26

TV signal processor-Teletext decoder with embedded μ -Controller

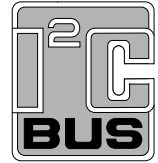
TDA935X/6X/8X series

GENERAL DESCRIPTION

The various versions of the TDA935X/6X/8X series combine the functions of a TV signal processor together with a μ -Controller and US Closed Caption decoder. Most versions have a Teletext decoder on board. The Teletext decoder has an internal RAM memory for 1 or 10 page text. The ICs are intended to be used in economy television receivers with 90° and 110° picture tubes.

The ICs have supply voltages of 8 V and 3.3 V and they are mounted in S-DIP envelope with 64 pins.

The features are given in the following feature list. The differences between the various ICs are given in the table on page 4.



FEATURES

TV-signal processor

- Multi-standard vision IF circuit with alignment-free PLL demodulator
- Internal (switchable) time-constant for the IF-AGC circuit
- A choice can be made between versions with mono intercarrier sound FM demodulator and versions with QSS IF amplifier.
- The mono intercarrier sound versions have a selective FM-PLL demodulator which can be switched to the different FM sound frequencies (4.5/5.5/6.0/6.5 MHz). The quality of this system is such that the external band-pass filters can be omitted.
- Source selection between 'internal' CVBS and external CVBS or Y/C signals
- Integrated chrominance trap circuit
- Integrated luminance delay line with adjustable delay time
- Asymmetrical 'delay line type' peaking in the luminance channel
- Black stretching for non-standard luminance signals
- Integrated chroma band-pass filter with switchable centre frequency
- Only one reference (12 MHz) crystal required for the μ -Controller, Teletext- and the colour decoder
- PAL/NTSC or multi-standard colour decoder with automatic search system
- Internal base-band delay line
- RGB control circuit with 'Continuous Cathode Calibration', white point and black level off set adjustment so that the colour temperature of the dark and the light parts of the screen can be chosen independently.
- Linear RGB or YUV input with fast blanking for external RGB/YUV sources. The Text/OSD signals are internally supplied from the μ -Controller/Teletext decoder
- Contrast reduction possibility during mixed-mode of OSD and Text signals
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Vertical count-down circuit
- Vertical driver optimized for DC-coupled vertical output stages
- Horizontal and vertical geometry processing
- Horizontal and vertical zoom function for 16 : 9 applications
- Horizontal parallelogram and bow correction for large screen picture tubes
- Low-power start-up of the horizontal drive circuit

TV signal processor-Teletext decoder with embedded μ -Controller

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μ -Controller

- 80C51 μ -controller core standard instruction set and timing
- 1 μ s machine cycle
- 32 - 128Kx8-bit late programmed ROM
- 3 - 12Kx8-bit Auxiliary RAM (shared with Display and Acquisition)
- Interrupt controller for individual enable/disable with two level priority
- Two 16-bit Timer/Counter registers
- WatchDog timer
- Auxiliary RAM page pointer
- 16-bit Data pointer
- IDLE and Power Down (PD) mode
- 14 bits PWM for Voltage Synthesis Tuning
- 8-bit A/D converter
- 4 pins which can be programmed as general I/O pin, ADC input or PWM (6-bit) output

Data Capture

- Text memory for 1 or 10 pages
- In the 10 page versions inventory of transmitted Teletext pages stored in the Transmitted Page Table (TPT) and Subtitle Page Table (SPT)
- Data Capture for US Closed Caption
- Data Capture for 525/625 line WST, VPS (PDC system A) and Wide Screen Signalling (WSS) bit decoding
- Automatic selection between 525 WST/625 WST
- Automatic selection between 625 WST/VPS on line 16 of VBI
- Real-time capture and decoding for WST Teletext in Hardware, to enable optimized μ -processor throughput
- Automatic detection of FASTEXT transmission
- Real-time packet 26 engine in Hardware for processing accented, G2 and G3 characters
- Signal quality detector for video and WST/VPS data types
- Comprehensive teletext language coverage
- Full Field and Vertical Blanking Interval (VBI) data capture of WST data

Display

- Teletext and Enhanced OSD modes
- Features of level 1.5 WST and US Close Caption
- Serial and Parallel Display Attributes
- Single/Double/Quadruple Width and Height for characters
- Scrolling of display region
- Variable flash rate controlled by software
- Enhanced display features including overlining, underlining and italics
- Soft colours using CLUT with 4096 colour palette
- Globally selectable scan lines per row (9/10/13/16) and character matrix [12x10, 12x13, 12x16 (VxH)]
- Fringing (Shadow) selectable from N-S-E-W direction
- Fringe colour selectable
- Meshing of defined area
- Contrast reduction of defined area
- Cursor
- Special Graphics Characters with two planes, allowing four colours per character
- 32 software redefinable On-Screen display characters
- 4 WST Character sets (G0/G2) in single device (e.g. Latin, Cyrillic, Greek, Arabic)
- G1 Mosaic graphics, Limited G3 Line drawing characters
- WST Character sets and Closed Caption Character set in single device

TV signal processor-Teletext decoder with
embedded μ -Controller

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FUNCTIONAL DIFFERENCE BETWEEN THE VARIOUS IC VERSIONS

IC VERSION (TDA)	9350	9351	9352	9353	9360	9361	9362	9363	9364	9365	9366	9367	9380	9381	9382	9383	9384	9385	9386	9387	9388
TV range	90°	90°	90°	110°	90°	90°	110°	110°	110°	110°	90°	90°	90°	90°	90°	110°	110°	110°	110°	90°	110°
Mono intercarrier multi-standard sound demodulator (4.5 - 6.5 MHz) with switchable centre frequency	√	√		√	√	√	√	√					√	√		√	√			√	√
Audio switch	√	√		√	√	√	√	√					√	√		√	√			√	√
Automatic Volume Levelling	√	√	√		√	√					√	√	√	√	√					√	√
Automatic Volume Levelling or subcarrier output (for comb filter applications)				√			√	√	√	√						√	√	√	√		
QSS sound IF amplifier with separate input and AGC circuit			√						√	√	√	√			√			√	√		
AM sound demodulator without extra reference circuit										√									√		
PAL decoder	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√		
SECAM decoder		√	√	√		√		√		√		√		√	√		√		√		
NTSC decoder	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
Horizontal geometry (E-W)				√			√	√	√	√						√	√	√	√		√
Horizontal and Vertical Zoom				√			√	√	√	√						√	√	√	√		√
ROM size	32-64 k	32-64 k	32-64 k	32-64 k	32-64 k	32-64 k	64-128k	64-128k	64-128k	64-128k	64-128k	64-128k	16-64 k	16-64 k	16-64 k	16-64 k	16-64 k	16-64 k	16-64 k	16-64 k	16-64 k
User RAM size	1 k	1 k	1 k	1 k	2 k	2 k	2 k	2 k	2 k	2 k	2 k	2 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k
Teletext	1 page	1 page	1 page	1 page	10 page	10 page	10 page	10 page	10 page	10 page	10 page	10 page									
Closed captioning	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√

TV signal processor-Teletext decoder with embedded μ -Controller

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltages	–	8.0/3.3	–	V
I_P	supply current	–	tbh	–	mA
Input voltages					
$V_{iVIF(rms)}$	video IF amplifier sensitivity (RMS value)	–	35	–	μ V
$V_{iSIF(rms)}$	QSS sound IF amplifier sensitivity (RMS value)	–	60	–	μ V
$V_{iAUDIO(rms)}$	external audio input (RMS value)	–	500	–	mV
$V_{iCVBS(p-p)}$	external CVBS/Y input (peak-to-peak value)	–	1.0	–	V
$V_{iCHROMA(p-p)}$	external chroma input voltage (burst amplitude) (peak-to-peak value)	–	0.3	–	V
$V_{iRGB(p-p)}$	RGB inputs (peak-to-peak value)	–	0.7	–	V
$V_{iYIN(p-p)}$	luminance input signal (peak-to-peak value)	–	1.4	–	V
$V_{iUVIN(p-p)}$	U/V input signal (peak-to-peak value)	–	1.33/1.05	–	V
Output signals					
$V_{o(IFVO)(p-p)}$	demodulated CVBS output (peak-to-peak value)	–	2.5	–	V
$V_{o(QSSO)(rms)}$	sound IF intercarrier output in QSS versions (RMS value)	–	100	–	mV
$V_{o(AMOUT)(rms)}$	demodulated AM sound output in QSS versions (RMS value)	–	500	–	mV
$I_{o(AGCOUT)}$	tuner AGC output current range	0	–	5	mA
$V_{oRGB(p-p)}$	RGB output signal amplitudes (peak-to-peak value)	–	2.0	–	V
I_{oHOUT}	horizontal output current	10	–	–	mA
I_{oVERT}	vertical output current (peak-to-peak value)	1	–	–	mA
I_{oEWD}	EW drive output current	1.2	–	–	mA

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BLOCK DIAGRAM

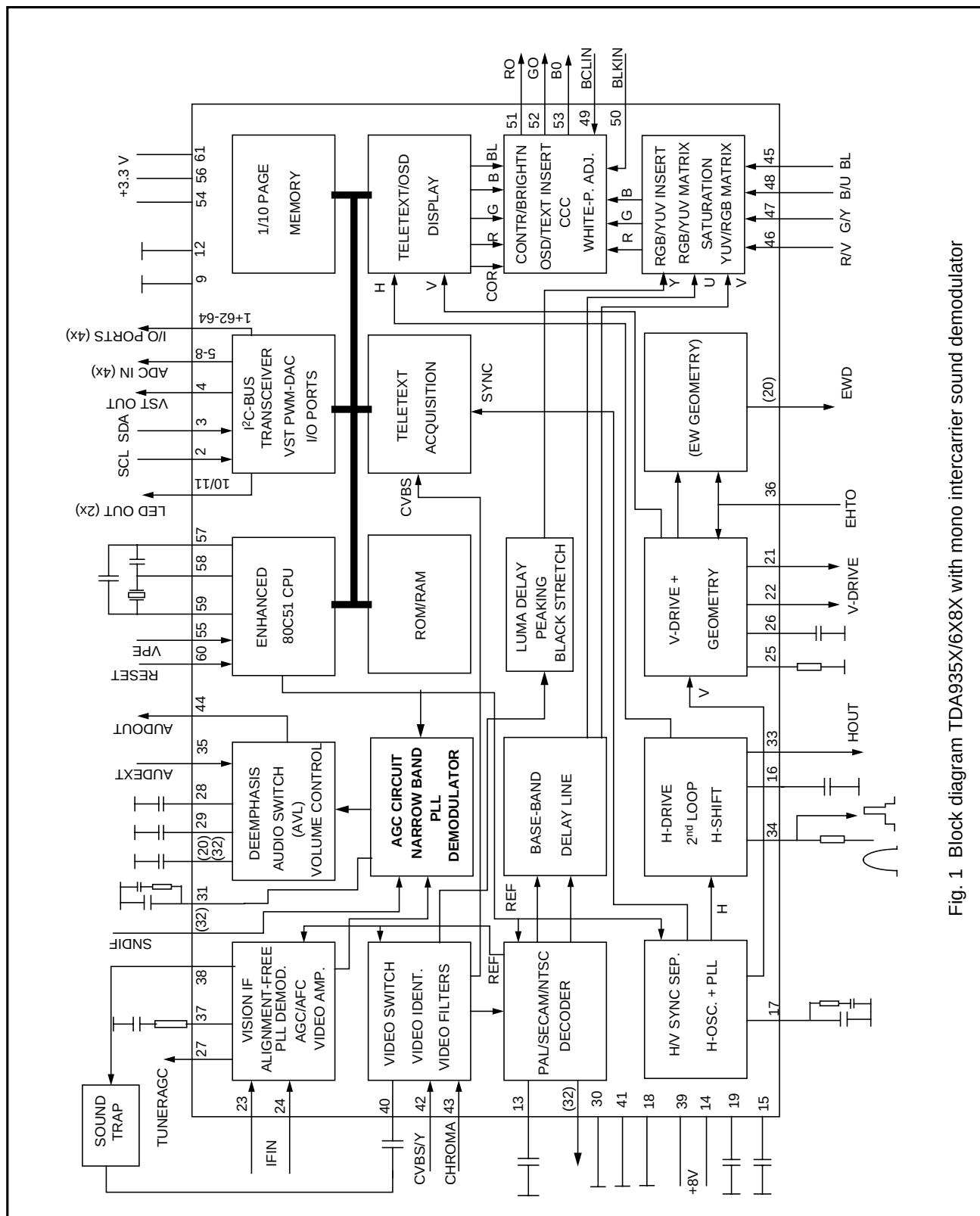


Fig. 1 Block diagram TDA935X/6X8X with mono intercarrier sound demodulator

TV signal processor-Teletext decoder with
embedded μ -Controller

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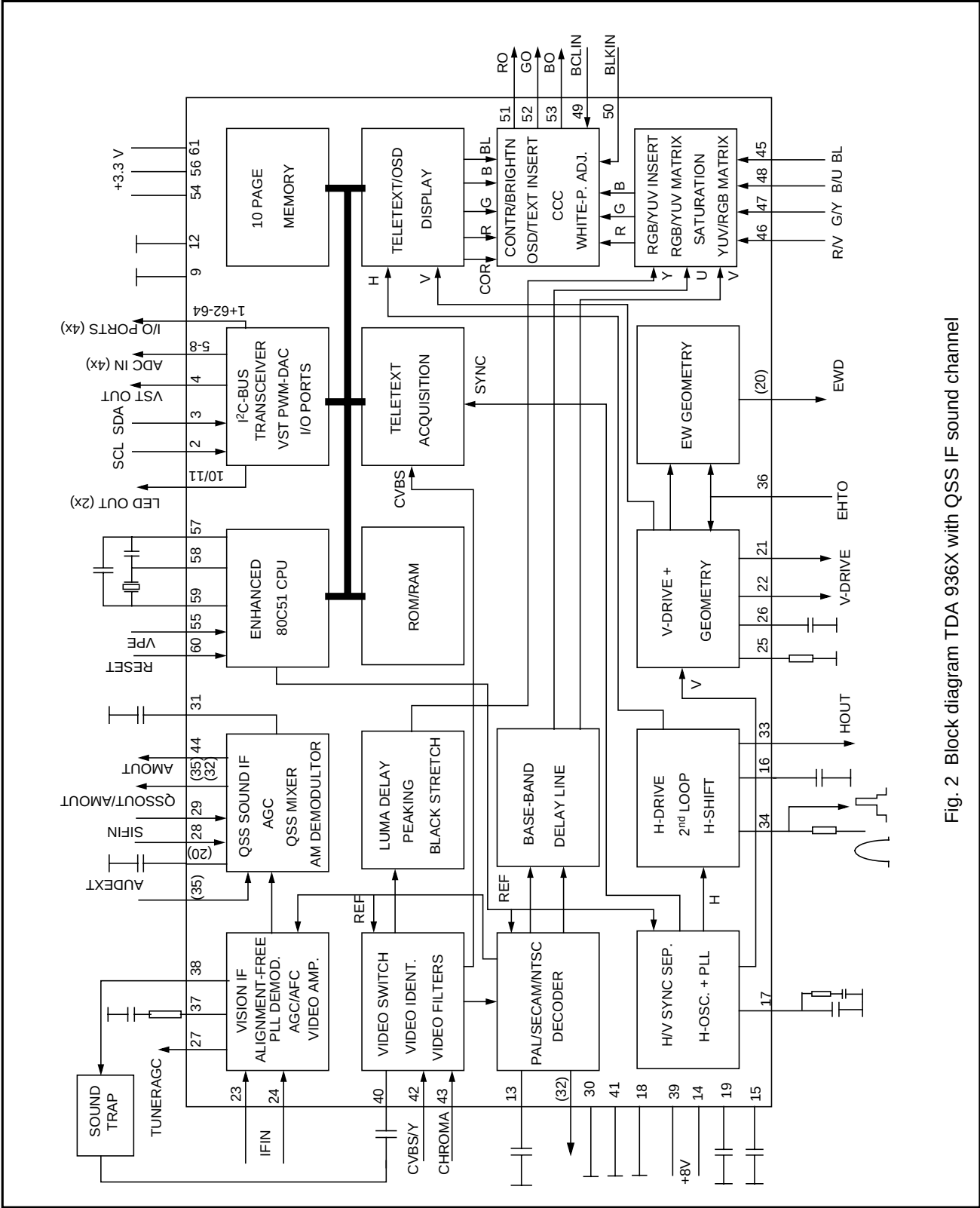


Fig. 2 Block diagram TDA 936X with QSS IF sound channel

TV signal processor-Teletext decoder with embedded μ -Controller

TDA935X/6X/8X series

PINNING

SYMBOL	PIN	DESCRIPTION
P1.3/T1	1	port 1.3 or Counter/Timer 1 input
P1.6/SCL	2	port 1.6 or I ² C-bus clock line
P1.7/SDA	3	port 1.7 or I ² C-bus data line
P2.0/TPWM	4	port 2.0 or Tuning PWM output
P3.0/ADC0	5	port 3.0 or ADC0 input
P3.1/ADC1	6	port 3.1 or ADC1 input
P3.2/ADC2	7	port 3.2 or ADC2 input
P3.3/ADC3	8	port 3.3 or ADC3 input
VSSC/P	9	digital ground for μ -Controller core and periphery
P0.5	10	port 0.5 (8 mA current sinking capability for direct drive of LEDs)
P0.6	11	port 0.6 (8 mA current sinking capability for direct drive of LEDs)
VSSA	12	analog ground of Teletext decoder and digital ground of TV-processor
SECPLL	13	SECAM PLL decoupling
VP2	14	2 nd supply voltage TV-processor (+8V)
DECDIG	15	decoupling digital supply of TV-processor
PH2LF	16	phase-2 filter
PH1LF	17	phase-1 filter
GND3	18	ground 3 for TV-processor
DECBG	19	bandgap decoupling
AVL/EWD ⁽¹⁾	20	Automatic Volume Levelling /East-West drive output
VDRB	21	vertical drive B output
VDRA	22	vertical drive A output
IFIN1	23	IF input 1
IFIN2	24	IF input 2
IREF	25	reference current input
VSC	26	vertical sawtooth capacitor
TUNERAGC	27	tuner AGC output
AUDEEM/SIFIN1 ⁽¹⁾	28	audio deemphasis or SIF input 1
DECSDEM/SIFIN2 ⁽¹⁾	29	decoupling sound demodulator or SIF input 2
GND2	30	ground 2 for TV processor
SNDPLL/SIFAGC ⁽¹⁾	31	narrow band PLL filter /AGC sound IF
AVL/SNDIF/REF0/ AMOUT ⁽¹⁾	32	Automatic Volume Levelling / sound IF input / subcarrier reference output /AM output (non controlled)
HOUT	33	horizontal output
FBISO	34	flyback input/sandcastle output
AUDEXT/ QSSO/AMOUT ⁽¹⁾	35	external audio input /QSS intercarrier out /AM audio output (non controlled)
EHTO	36	EHT/overvoltage protection input
PLLIF	37	IF-PLL loop filter
IFVO/SVO	38	IF video output / selected CVBS output
VP1	39	main supply voltage TV-processor (+8 V)
CVBSINT	40	internal CVBS input
GND1	41	ground 1 for TV-processor

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SYMBOL	PIN	DESCRIPTION
CVBS/Y	42	external CVBS/Y input
CHROMA	43	chrominance input (SVHS)
AUDOUT /AMOUT ⁽¹⁾	44	audio output /AM audio output (volume controlled)
INSSW2	45	2 nd RGB / YUV insertion input
R2/VIN	46	2 nd R input / V (R-Y) input
G2/YIN	47	2 nd G input / Y input
B2/UIN	48	2 nd B input / U (B-Y) input
BCLIN	49	beam current limiter input/V-guard input
BLKIN	50	black current input
RO	51	Red output
GO	52	Green output
BO	53	Blue output
VDDA	54	analog supply of Teletext decoder and digital supply of TV-processor (3.3 V)
VPE	55	OTP Programming Voltage
VDDC	56	digital supply to core (3.3 V)
OSCGND	57	oscillator ground supply
XTALIN	58	crystal oscillator input
XTALOUT	59	crystal oscillator output
RESET	60	reset
VDDP	61	digital supply to periphery (+3.3 V)
P1.0/INT1	62	port 1.0 or external interrupt 1 input
P1.1/T0	63	port 1.1 or Counter/Timer 0 input
P1.2/INT0	64	port 1.2 or external interrupt 0 input

Note

1. The function of pin 20, 28, 29, 31, 32, 35 and 44 is dependent on the IC version (mono intercarrier FM demodulator / QSS IF amplifier and East-West output or not) and on some software control bits. The valid combinations are given in table 1.

Table 1 Pin functions for various versions

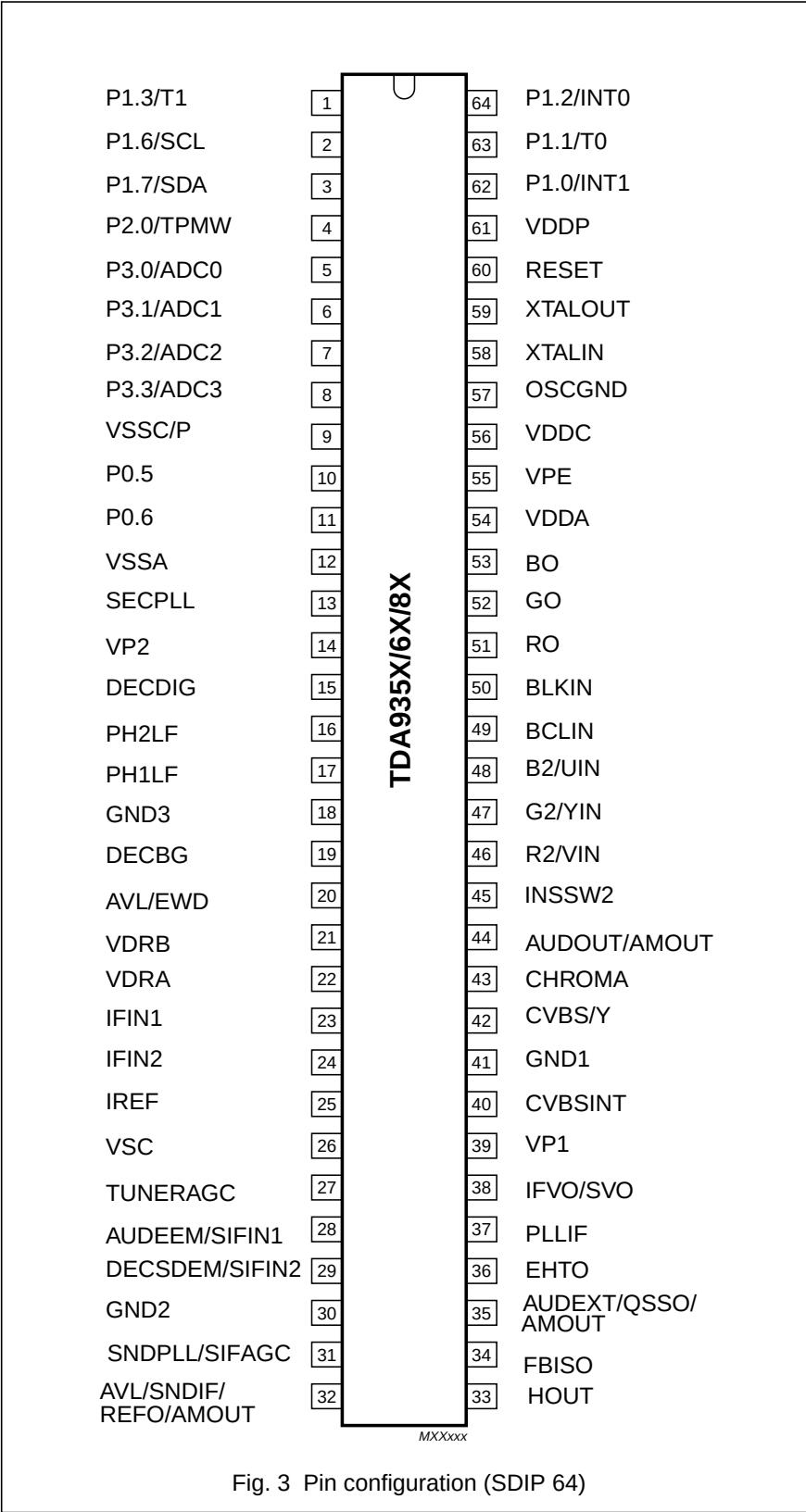
IC version	FM-PLL version				QSS version					
East-West Y/N	N		Y		N			Y		
CMB1/CMB0 bits	00	01/10/11	00	01/10/11	00	01/10/11		00	01/10/11	
AM bit	–	–	–	–	–	0	1	–	0	1
Pin 20	AVL		EWD		AVL			EWD		
Pin 28	AUDEEM				SIFIN1					
Pin 29	DECSDEM				SIFIN2					
Pin 31	SNDPLL				SIFAGC					
Pin 32	SNDIF ⁽¹⁾	REFO	AVL/SNDIF ⁽¹⁾	REFO	AMOUT	REFO		AMOUT	REFO	
Pin 35	AUDEXT				AUDEXT	QSSO	AMOUT	AUDEXT	QSSO	AMOUT
Pin 44	AUDOUT				controlled AM or audio out					

Note

1. When additional (external) selectivity is required for FM-PLL system pin 32 can be used as sound IF input. This function is selected by means of SIF bit in subaddress 21H.

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TV signal processor-Teletext decoder with embedded μ -Controller

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FUNCTIONAL DESCRIPTION OF THE MICRO-CONTROLLER/TEXT DECODER

Block Diagram

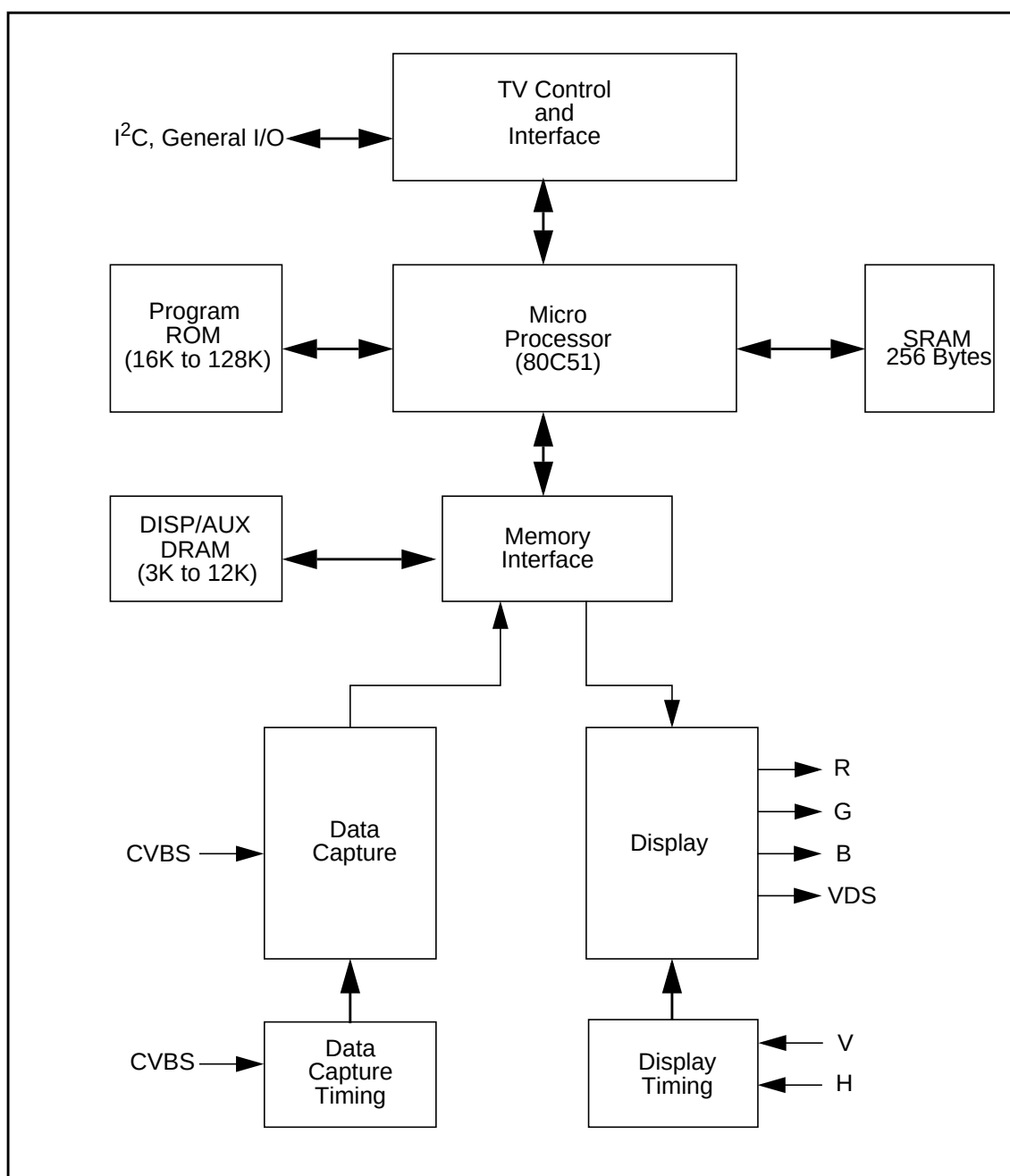


Figure 4 Top level architecture

TV signal processor-Teletext decoder with embedded μ -Controller

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Microcontroller

The functionality of the microcontroller used on the device is described here with reference to the industry standard 80C51 microcontroller. A full description of its functionality can be found in the "80C51 Based 8-Bit Microcontrollers - Philips Semiconductors (ref. IC20)" (Reference [1])

Memory Organisation

The device has the capability of a maximum of 128K PROGRAM ROM and 12K DATA RAM internally.

ROM BANK SWITCHING

Devices with up to 64K Program ROM have a continuous address space. Devices with over 64K Program ROM use ROM bank switching. The 128K version is arranged in four banks of 32K. One of the 32K banks is common and is always addressable. The other three banks(Bank0,Bank1,Bank2) can be accessed by selecting the right bank via the SFR ROMBK bits 1/0.

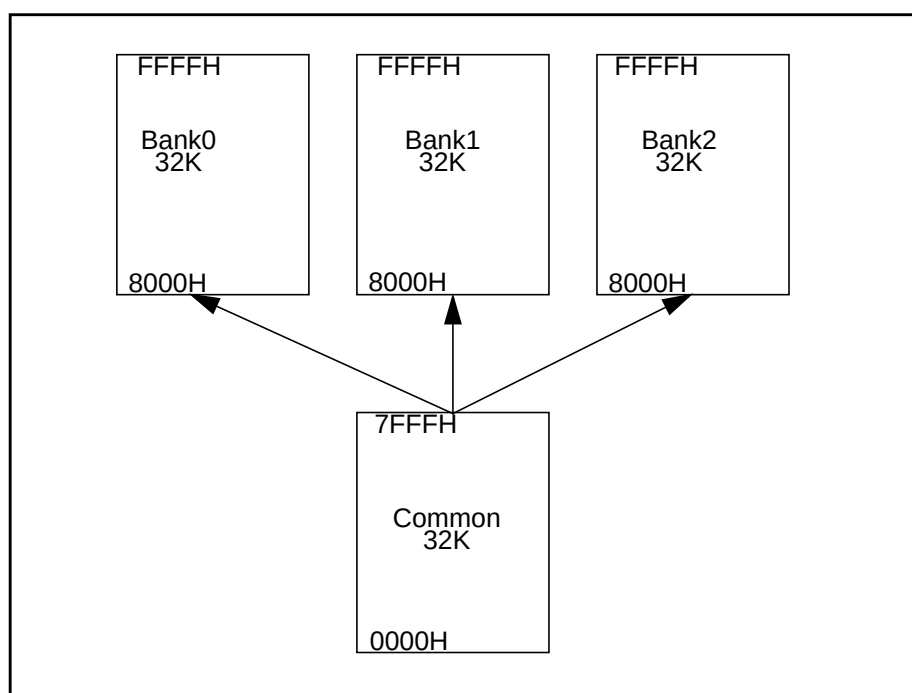


Figure 5 ROM Bank Switching memory map

ROMBK<2:0>	0 to 32K	32K to 64K
00	Common	Bank0
01	Common	Bank1
10	Common	Bank2
11	Reserved	Reserved

Table 2 ROM Bank Selection

TV signal processor-Teletext decoder with
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Security Bits - Program and Verify

TDA935X/6X/8X devices have three sets of security bits, one set for each of the three One Time Programmable memories, i.e. Program ROM, Character ROM and Packet 26 ROM. The security bits are used to prevent the ROM from being overwritten once programmed, and also the contents being verified once programmed. The security bits are one-time programmable and **cannot** be erased.

The TDA935X/6X/8X memory and security bits are structured as shown in Figure 6. The security bits are set as shown in Figure 7 for production programmed devices and are set as shown in Figure 8 for production blank devices.

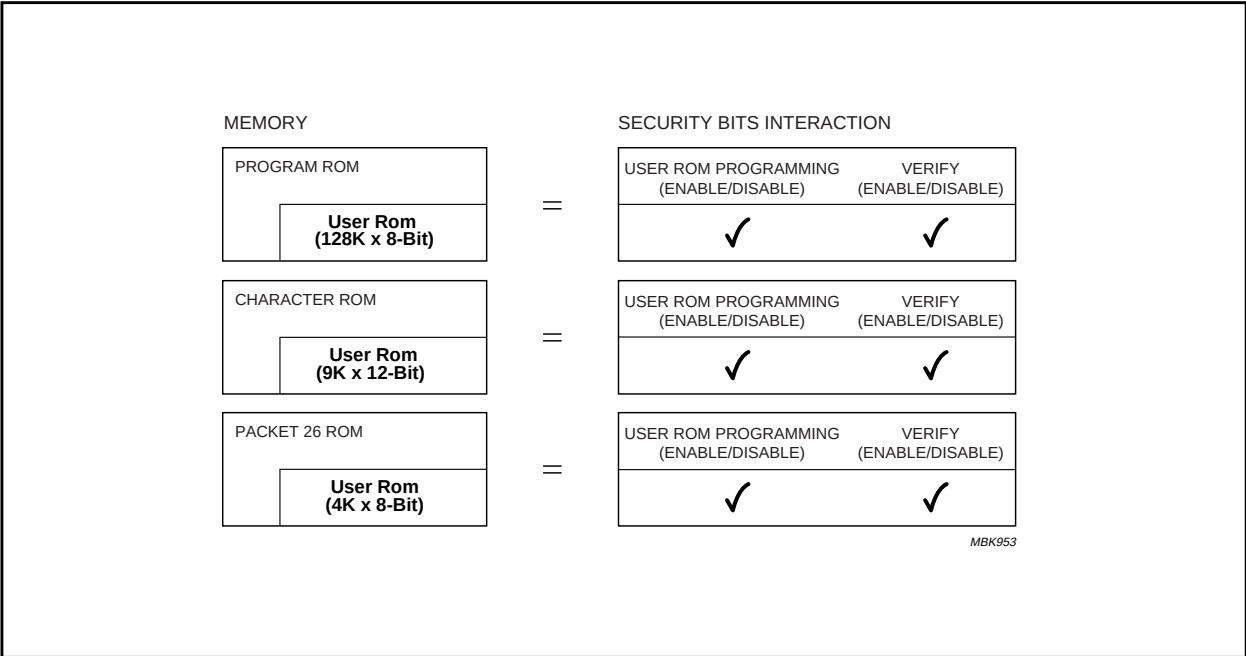


Figure 6 Memory and security bit structures

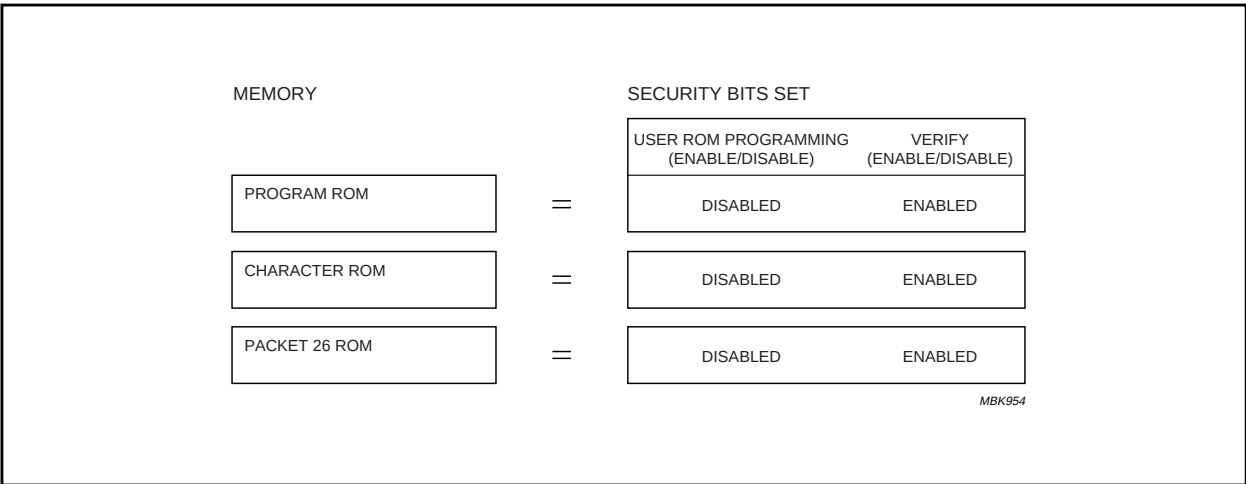


Figure 7 Security bits for production devices

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

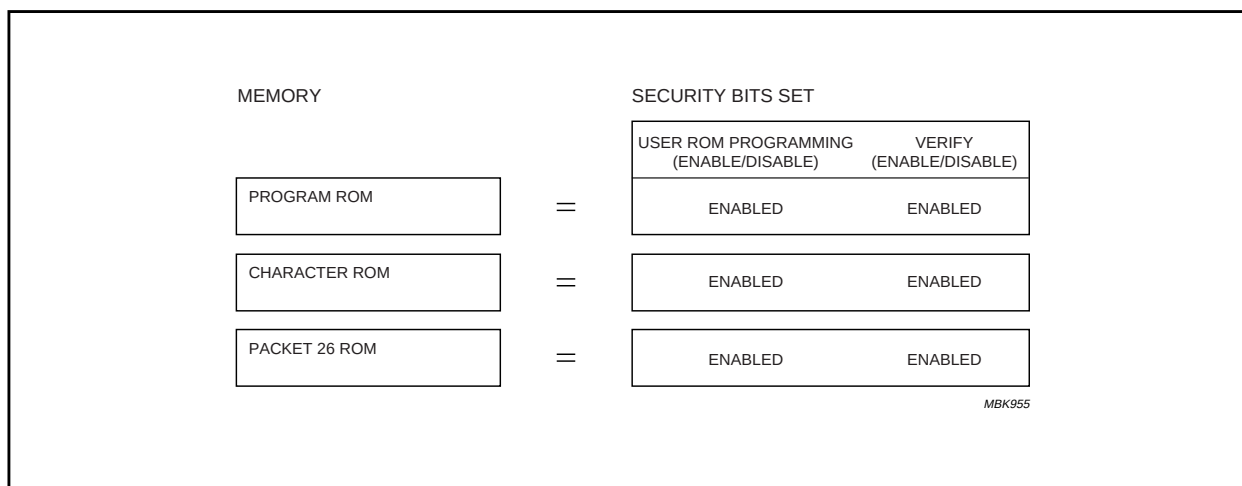


Figure 8 Security bits for production blank devices

RAM ORGANISATION

The Internal Data RAM is organised into two areas, Data Memory and Special Function Registers (SFR's) as shown in Figure 9.

Data Memory

The Data memory is 256 x 8 bits wide (byte) and occupies the address range 00h to 255h when using indirect addressing and 00h to 127h when using Direct addressing. The SFRs occupy the address range 128 to 255 and are accessible using Direct addressing only.

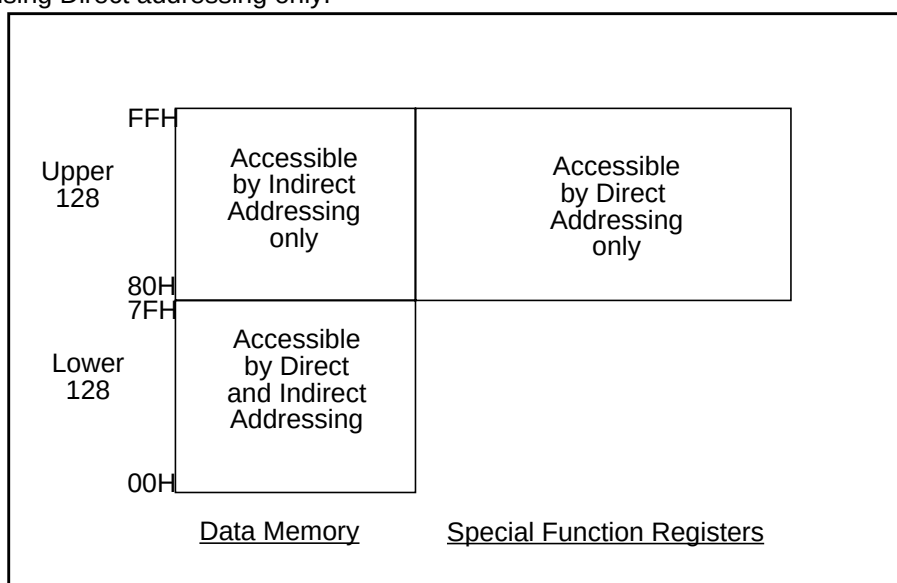


Figure 9 Internal Data Memory

The lower 128 Bytes of Data memory are mapped as shown in Figure 10. The lowest 24 bytes are grouped into 4 banks of 8 registers, the next 16 bytes above the register banks form a block of bit addressable memory space.

TV signal processor-Teletext decoder with embedded μ -Controller

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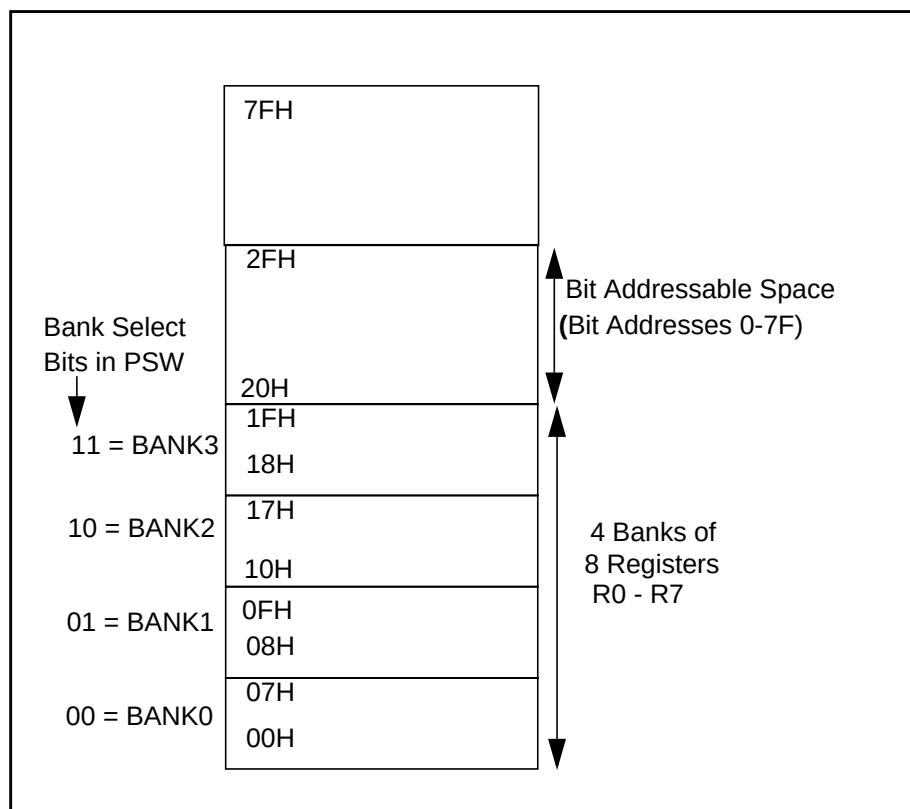


Figure 10 Lower 128 Bytes of Internal RAM

The upper 128 bytes is not allocated for any special area or functions.

SFR Memory

The Special Function Register (SFR) space is used for Port latches, timer, peripheral control, acquisition control, display control, etc. These register can only be accessed by direct addressing. Sixteen of the addresses in the SFR space are both byte and bit-addressable. The bit-addressable SFR's are those whose address ends in 0H or 8H. A summary of the SFR map in address order is shown in Table 3..

ADD	R/W	Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
80H	R/W	P0	-	P0<6>	P0<5>	-	-	-	-	-
81H	R/W	SP	SP<7>	SP<6>	SP<5>	SP<4>	SP<3>	SP<2>	SP<1>	SP<0>
82H	R/W	DPL	DPL<7>	DPL<6>	DPL<5>	DPL<4>	DPL<3>	DPL<2>	DPL<1>	DPL<0>
83H	R/W	DPH	DPH<7>	DPH<6>	DPH<5>	DPH<4>	DPH<3>	DPH<2>	DPH<1>	DPH<0>
87H	R/W	PCON	0	ARD	RFI	WLE	GF1	GF0	PD	IDL
88H	R/W	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89H	R/W	TMOD	GATE	C/ $\bar{T}$	M1	M0	GATE	C/ $\bar{T}$	M1	M0
8AH	R/W	TL0	TL0<7>	TL0<6>	TL0<5>	TL0<4>	TL0<3>	TL0<2>	TL0<1>	TL0<0>
8BH	R/W	TL1	TL1<7>	TL1<6>	TL1<5>	TL1<4>	TL1<3>	TL1<2>	TL1<1>	TL1<0>

Table 3 SFR Map

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

ADD	R/W	Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
8CH	R/W	TH0	TH0<7>	TH0<6>	TH0<5>	TH0<4>	TH0<3>	TH0<2>	TH0<1>	TH0<0>
8DH	R/W	TH1	TH1<7>	TH1<6>	TH1<5>	TH1<4>	TH1<3>	TH1<2>	TH1<1>	TH1<0>
90H	R/W	P1	P1<7>	P1<6>	-	-	P1<3>	P1<2>	P1<1>	P1<0>
96H	R/W	P0CFGA	-	P0CFGA<6>	P0CFGA<5>	-	-	-	-	-
97H	R/W	P0CFGB	-	P0CFGB<6>	P0CFGB<5>	-	-	-	-	-
98H	R/W	SADB	0	0	0	DC COMP	SAD<3>	SAD<2>	SAD<1>	SAD<0>
9EH	R/W	P1CFGA	P1CFGA<7>	P1CFGA<6>	-	-	P1CFGA<3>	P1CFGA<2>	P1CFGA<1>	P1CFGA<0>
9FH	R/W	P1CFGB	P1CFGB<7>	P1CFGB<6>	-	-	P1CFGB<3>	P1CFGB<2>	P1CFGB<1>	P1CFGB<0>
A0H	R/W	P2	-	-	-	-	-	-	-	P2<0>
A6H	R/W	P2CFGA	-	-	-	-	-	-	-	P2CFGA<0>
A7H	R/W	P2CFGB	-	-	-	-	-	-	-	P2CFGB<0>
A8H	R/W	IE	EA	EBUSY	ES2	ECC	ET1	EX1	ET0	EX0
B0H	R/W	P3	-	-	-	-	P3<3>	P3<2>	P3<1>	P3<0>
B2H	R/W	TXT18	NOT<3>	NOT<2>	NOT<1>	NOT<0>	0	0	BS<1>	BS<0>
B3H	R/W	TXT19	TEN	TC<2>	TC<1>	TC<0>	0	0	TS<1>	TS<0>
B4H	R/W	TXT20	DRCS ENABLE	OSD PLANES	0	0	OSD LANG ENABLE	OSD LAN<2>	OSD LAN<1>	OSD LAN<0>
B5H	R/W	TXT21	DISP LINE<1>	DISP LINES<0>	CHAR SIZE<1>	CHAR SIZE<0>	0	CC ON	I2C PORT0	CC/TXT
B7H	R/W	CCLIN	0	0	0	CS<4>	CS<3>	CS<2>	CS<1>	CS<0>
B8H	R/W	IP	0	PBUSY	PES2	PCC	PT1	PX1	PT0	PX0
B9H	R/W	TXT17	0	FORCE ACQ<1>	FORCE ACQ<0>	FORCE DISP<1>	FORCE DISP<0>	SCREEN COL<2>	SCREEN COL<1>	SCREEN COL<0>
BAH	R	WSS1	0	0	0	WSS<3:0> ERROR	WSS<3>	WSS<2>	WSS<1>	WSS<0>
BBH	R	WSS2	0	0	0	WSS<7:4> ERROR	WSS<7>	WSS<6>	WSS<5>	WSS<4>
BCH	R	WSS3	WSS<13:11> ERROR	WSS<13>	WSS<12>	WSS<11>	WSS<10:8> ERROR	WSS<10>	WSS<9>	WSS<8>
BEH	R/W	P3CFGA	-	-	-	-	P3CFGA<3>	P3CFGA<2>	P3CFGA<1>	P3CFGA<0>
BFH	R/W	P3CFGB	-	-	-	-	P3CFGB<3>	P3CFGB<2>	P3CFGB<1>	P3CFGB<0>
C0H	R/W	TXT0	X24 POSN	DISPLAY X24	-	DISABLE HEADER ROLL	DISPLAY STATUS ROW ONLY	-	VPS ON	INV ON
C1H	R/W	TXT1	EXT PKT OFF	8 BIT	ACQ OFF	X26 OFF	FULL FIELD	-	-	-
C2H	R/W	TXT2	(Reserved) 0	REQ<3>	REQ<2>	REQ<1>	REQ<0>	SC<2>	SC<1>	SC<0>
C3H	W	TXT3	-	-	-	PRD<4>	PRD<3>	PRD<2>	PRD<1>	PRD<0>
C4H	R/W	TXT4	OSD BANK ENABLE	QUAD WIDTH ENABLE	EAST/WEST	DISABLE DOUBLE HEIGHT	B MESH ENABLE	C MESH ENABLE	TRANS ENABLE	SHADOW ENABLE
C5H	R/W	TXT5	BKGND OUT	BKGND IN	CORB OUT	CORB IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN
C6H	R/W	TXT6	BKGND OUT	BKGND IN	CORB OUT	CORB IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN

Table 3 SFR Map

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

ADD	R/W	Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
C7H	R/W	TXT7	STATUS ROW TOP	CURSOR ON	REVEAL	BOTTOM/TOP	DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
C8H	R/W	TXT8	(Reserved) 0	FLICKER STOP ON	(Reserved) 0	DISABLE SPANISH	PKT 26 RECEIVED	WSS RECEIVED	WSS ON	(Reserved) 0
C9H	R/W	TXT9	CURSOR FREEZE	CLEAR MEMORY	A0	R<4>	R<3>	R<2>	R<1>	R<0>
CAH	R/W	TXT10	0	0	C<5>	C<4>	C<3>	C<2>	C<1>	C<0>
CBH	R/W	TXT11	D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
CCH	R	TXT12	525/625 SYNC	SPANISH	ROM VER<3>	ROM VER<2>	ROM VER<1>	ROM VER<0>	1	VIDEO SIGNAL QUALITY
CDH	R/W	TXT14	0	0	0	(Reserved) 0	PAGE<3>	PAGE<2>	PAGE<1>	PAGE<0>
CEH	R/W	TXT15	0	0	0	(Reserved) 0	BLOCK<3>	BLOCK<2>	BLOCK<1>	BLOCK<0>
D0H	R/W	PSW	C	AC	F0	RS1	RS0	OV	-	P
D2H	R/W	TDACL	TD<7>	TD<6>	TD<5>	TD<4>	TD<3>	TD<2>	TD<1>	TD<0>
D3H	R/W	TDACH	TPWE	1	TD<13>	TD<12>	TD<11>	TD<10>	TD<9>	TD<8>
D5H	R/W	PWM0	PW0E	1	PW0V<5>	PW0V<4>	PW0V<3>	PW0V<2>	PW0V<1>	PW0V<0>
D6H	R/W	PWM1	PW1E	1	PW1V<5>	PW1V<4>	PW1V<3>	PW1V<2>	PW1V<1>	PW1V<0>
D7H	R	CCDAT1	CCD1<7>	CCD1<6>	CCD1<5>	CCD1<4>	CCD1<3>	CCD1<2>	CCD1<1>	CCD1<0>
D8H	R/W	SICON	CR<2>	ENSI	STA	STO	SI	AA	CR<1>	CR<0>
D9H	R	SISTA	STAT<4>	STAT<3>	STAT<2>	STAT<1>	STAT<0>	0	0	0
DAH	R/W	SIDAT	DAT<7>	DAT<6>	DAT<5>	DAT<4>	DAT<3>	DAT<2>	DAT<1>	DAT<0>
DBH	R/W	S1ADR	ADR<6>	ADR<5>	ADR<4>	ADR<3>	ADR<2>	ADR<1>	ADR<0>	GC
DCH	R/W	PWM3	PW3E	1	PW3V<5>	PW3V<4>	PW3V<3>	PW3V<2>	PW3V<1>	PW3V<0>
E0H	R/W	ACC	ACC<7>	ACC<6>	ACC<5>	ACC<4>	ACC<3>	ACC<2>	ACC<1>	ACC<0>
E4H	R/W	PWM2	PW2E	1	PW2V<5>	PW2V<4>	PW2V<3>	PW2V<2>	PW2V<1>	PW2V<0>
E7H	R	CCDAT2	CCD2<7>	CCD2<6>	CCD2<5>	CCD2<4>	CCD2<3>	CCD2<2>	CCD2<1>	CCD2<0>
E8H	R/W	SAD	VHI	CH<1>	CH<0>	ST	SAD<7>	SAD<6>	SAD<5>	SAD<4>
F0H	R/W	B	B<7>	B<6>	B<5>	B<4>	B<3>	B<2>	B<1>	B<0>
F7H	W	WDTKEY	WKEY<7>	WKEY<6>	WKEY<5>	WKEY<4>	WKEY<3>	WKEY<2>	WKEY<1>	WKEY<0>
F8H	R/W	TXT13	VPS RECEIVED	PAGE CLEARING	525 DISPLAY	525 TEXT	625 TEXT	PKT 8/30	FASTEXT	(Reserved) 0
FAH	R/W	XRAMP	XRAMP<7>	XRAMP<6>	XRAMP<5>	XRAMP<4>	XRAMP<3>	XRAMP<2>	XRAMP<1>	XRAMP<0>
FBH	R/W	ROMBK	STANDBY	0	0	0	0	0	ROMBK<1>	ROMBK<0>
FFH	R/W	WDT	WDV<7>	WDV<6>	WDV<5>	WDV<4>	WDV<3>	WDV<2>	WDV<1>	WDV<0>

Table 3 SFR Map

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

The description of each of the SFR bits is shown in Table 4, The table has the SFR's in alphabetical order.

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
ACC	ACC<7>	ACC<6>	ACC<5>	ACC<4>	ACC<3>	ACC<2>	ACC<1>	ACC<0>	00H
ACC<7:0>	Accumulator value								
B	B<7>	B<6>	B<5>	B<4>	B<3>	B<2>	B<1>	B<0>	00H
B<7:0>	B Register value								
CCDAT1	CCD1<7>	CCD1<6>	CCD1<5>	CCD1<4>	CCD1<3>	CCD1<2>	CCD1<1>	CCD1<0>	00H
CCD1<7:0>	Closed Caption first data byte								
CCDAT2	CCD2<7>	CCD2<6>	CCD2<5>	CCD2<4>	CCD2<3>	CCD2<2>	CCD2<1>	CCD2<0>	00H
CCD2<7:0>	Closed Caption second data byte								
CCLIN	0	0	0	CS<4>	CS<3>	CS<2>	CS<1>	CS<0>	15H
CS<4:0>	Closed caption Slice line using 525 line number.								
DPH	DPH<7>	DPH<6>	DPH<5>	DPH<4>	DPH<3>	DPH<2>	DPH<1>	DPH<0>	00H
DPH<7:0>	Data Pointer High byte, used with DPL to address auxiliary memory								
DPL	DPL<7>	DPL<6>	DPL<5>	DPL<4>	DPL<3>	DPL<2>	DPL<1>	DPL<0>	00H
DPL<7:0>	Data pointer low byte, used with DPH to address auxiliary memory								
IE	EA	EBUSY	ES2	ECC	ET1	EX1	ET0	EX0	00H
EA	Disable all interrupts (0), or use individual interrupt enable bits (1)								
EBUSY	Enable BUSY interrupt								
ES2	Enable I ² C interrupt								
ECC	Enable Closed Caption interrupt								
ET1	Enable Timer 1 interrupt								
EX1	Enable external interrupt 1								
ET0	Enable Timer 0 interrupt								
EX0	Enable External interrupt 0								
IP	0	PBUSY	PES2	PCC	PT1	PX1	PT0	PX0	00H
PBUSY	Priority EBUSY interrupt								
PES2	Priority ES2 Interrupt								
PCC	Priority ECC interrupt								
PT1	Priority Timer 1 interrupt								
PX1	Priority External Interrupt 1								
PT0	Priority Timer 0 interrupt								
PX0	Priority External Interrupt 0								
P0	-	P0<6>	P0<5>	-	-	-	-	-	FFH
P0<6:5>	Port 0 I/O register connected to external pins								
P1	P1<7>	P1<6>	-	-	P1<3>	P1<2>	P1<1>	P1<0>	FFH
P1<7:6,3:0>	Port 1 I/O register connected to external pins								
P2	-	-	-	-	-	-	-	P2<0>	FFH
P2<0>	Port 2 I/O register connected to external pins								

Table 4 SFR Bit description

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
P3	-	-	-	-	P3<3>	P3<2>	P3<1>	P3<0>	FFH
P3<3:0>	Port 3 I/O register connected to external ADC pins. Any combination of ADC input or PWM (P3<3:0>) output available via Software control.								
P0CFGA	-	P0CFGA<6>	P0CFGA<5>	-	-	-	-	-	FFH
P0CFGB	-	P0CFGB<6>	P0CFGB<5>	-	-	-	-	-	00H
P0CFGB<x>/P0CFGA<x> = 00	MODE 0 Open Drain								
P0CFGB<x>/P0CFGA<x> = 01	MODE 1 Quasi Bi-Directional								
P0CFGB<x>/P0CFGA<x> = 10	MODE2 High Impedance								
P0CFGB<x>/P0CFGA<x> = 11	MODE3 Push Pull								
P1CFGA	P1CFGA<7>	P1CFGA<6>	-	-	P1CFGA<3>	P1CFGA<2>	P1CFGA<1>	P1CFGA<0>	FFH
P1CFGB	P1CFGB<7>	P1CFGB<6>	-	-	P1CFGB<3>	P1CFGB<2>	P1CFGB<1>	P1CFGB<0>	00H
P1CFGB<x>/P1CFGA<x> = 00	MODE 0 Open Drain								
P1CFGB<x>/P1CFGA<x> = 01	MODE 1 Quasi Bi-Directional								
P1CFGB<x>/P1CFGA<x> = 10	MODE2 High Impedance								
P1CFGB<x>/P1CFGA<x> = 11	MODE3 Push Pull								
P2CFGA	-	-	-	-	-	-	-	P2CFGA<0>	FFH
P2CFGB	-	-	-	-	-	-	-	P2CFGB<0>	00H
P2CFGB<x>/P2CFGA<x> = 00	MODE 0 Open Drain								
P2CFGB<x>/P2CFGA<x> = 01	MODE 1 Quasi Bi-Directional								
P2CFGB<x>/P2CFGA<x> = 10	MODE2 High Impedance								
P2CFGB<x>/P2CFGA<x> = 11	MODE3 Push Pull								
P3CFGA	-	-	-	-	P3CFGA<3>	P3CFGA<2>	P3CFGA<1>	P3CFGA<0>	FFH
P3CFGB	-	-	-	-	P3CFGB<3>	P3CFGB<2>	P3CFGB<1>	P3CFGB<0>	00H
P3CFGB<x>/P3CFGA<x> = 00	MODE 0 Open Drain								
P3CFGB<x>/P3CFGA<x> = 01	MODE 1 Quasi Bi-directional								
P3CFGB<x>/P3CFGA<x> = 10	MODE2 High Impedance								
P3CFGB<x>/P3CFGA<x> = 11	MODE3 Push Pull								
PCON	-	ARD	RFI	WLE	GF1	GF0	PD	IDL	00H
ARD	Auxiliary RAM Disable, All MOVX instructions access the external data memory								
RFI	Disable ALE during internal access to reduce Radio Frequency Interference								
WLE	Watch Dog Timer enable								
GF1	General purpose flag								
GF0	General purpose flag								
PD	Power-down activation bit								
IDL	Idle mode activation bit								
PSW	C	AC	F0	RS<1>	RS<0>	OV	-	P	00H
C	Carry Bit								
AC	Auxiliary Carry bit								
F0	Flag 0, General purpose flag								

Table 4 SFR Bit description

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
RS<1:0>	Register Bank selector bits RS<1:0> = 00, Bank0 (00H - 07H) RS<1:0> = 01, Bank1 (08H - 0FH) RS<1:0> = 10, Bank2 (10H - 17H) RS<1:0> = 11, Bank3 (18H - 1FH)								
OV	Overflow flag								
P	Parity bit								
PWM0	PW0E	1	PW0V<5>	PW0V<4>	PW0V<3>	PW0V<2>	PW0V<1>	PW0V<0>	40H
PW0E	0 - Disable Pulse Width Modulator 0 1 - Enable Pulse Width Modulator 0								
PW0V<5:0>	Pulse Width Modulator high time								
PWM1	PW1E	1	PW1V<5>	PW1V<4>	PW1V<3>	PW1V<2>	PW1V<1>	PW1V<0>	40H
PW1E	0 - Disable Pulse Width Modulator 1 1 - Enable Pulse Width Modulator 1								
PW1V<5:0>	Pulse Width Modulator high time								
PWM2	PW2E	1	PW2V<5>	PW2V<4>	PW2V<3>	PW2V<2>	PW2V<1>	PW2V<0>	40H
PW2E	0 - Disable Pulse Width Modulator 2 1 - Enable Pulse Width Modulator 2								
PW2V<5:0>	Pulse Width Modulator high time								
PWM3	PW3E	1	PW3V<5>	PW3V<4>	PW3V<3>	PW3V<2>	PW3V<1>	PW3V<0>	40H
PW3E	0 - Disable Pulse Width Modulator 3 1 - Enable Pulse Width Modulator 3								
PW3V<5:0>	Pulse Width Modulator high time								
PW7V<5:0>	Pulse Width Modulator high time								
ROMBK	STANDBY	0	0	0	0	0	ROMBK<1>	ROMBK<0>	00H
STANDBY	0 - Stand-by mode inactive 1 - Stand-by mode active								
ROMBK<1:0>	ROM Bank selection ROMBK<1:0>=00, Bank0 ROMBK<1:0>=01, Bank1 ROMBK<1:0>=10, Bank2 ROMBK<1:0>=11, Reserved								
SIADR	ADR<6>	ADR<5>	ADR<4>	ADR<3>	ADR<2>	ADR<1>	ADR<0>	GC	00H
ADR<6:0>	I2C Slave Address								
GC	0 - Disable I ² C general call address 1 - Enable I ² C general call address								
SICON	CR<2>	ENSI	STA	STO	SI	AA	CR<1>	CR<0>	00H
CR<2:0>	Clock rate bits CR<2:0> = 000, 100KHz bit rate CR<2:0> = 001, 3.75kHz bit rate CR<2:0> = 010, 150KHz bit rate CR<2:0> = 011, 200KHz bit rate CR<2:0> = 100, 25KHz bit rate CR<2:0> = 101, 1.875KHz bit rate CR<2:0> = 110, 37.5KHz bit rate CR<2:0> = 111, 50KHz bit rate								

Table 4 SFR Bit description

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
ENSI	0 - Disable I ² C interface 1 - Enable I ² C interface								
STA	START flag. When this bit is set in slave mode, the hardware checks the I2C bus and generates a START condition if the bus is free or after the bus becomes free. If the device operates in master mode it will generate a repeated START condition.								
STO	STOP flag. If this bit is set in a master mode a STOP condition is generated. A STOP condition detected on the I2C bus clears this bit. This bit may also be set in slave mode in order to recover from an error condition. In this case no STOP condition is generated to the I2C bus, but the hardware releases the SDA and SCL lines and switches to the not selected receiver mode. The STOP flag is cleared by the hardware								
SI	Serial Interrupt flag. This flag is set and an interrupt request is generated, after any of the following events occur: -A START condition is generated in master mode. -The own slave address has been received during AA=1 -The general call address has been received while S1ADR.GC and AA=1 -A data byte has been received or transmitted in master mode (even if arbitration is lost) -A data byte has been received or transmitted as selected slave A STOP or START condition is received as selected slave receiver or transmitter While the SI flag is set, SCL remains LOW and the serial transfer is suspended.SI must be reset by software.								
AA	Assert Acknowledge flag. When this bit is set, an acknowledge is returned after any one of the following conditions -Own slave address is received. -General call address is received(S1ADR.GC=1) -A data byte is received, while the device is programmed to be a master receiver -A data byte is received, while the device is selected slave receiver When the bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own address or general call address is received.								
S1DAT	DAT<7>	DAT<6>	DAT<5>	DAT<4>	DAT<3>	DAT<2>	DAT<1>	DAT<0>	00H
DAT<7:0>	I ² C Data								
S1STA	STAT<4>	STAT<3>	STAT<2>	STAT<1>	STAT<0>	0	0	0	F8H
STAT<4:0>	I ² C Interface Status								
SAD	VHI	CH<1>	CH<0>	ST	SAD<7>	SAD<6>	SAD<5>	SAD<4>	00H
VHI	0 - Analogue input voltage less than DAC voltage 1 - Analogue input voltage greater then DAC voltage								
CH<1:0>	ADC Input channel select CH<1:0> = 00,ADC3 CH<1:0> = 01,ADC0 CH<1:0> = 10,ADC1 CH<1:0> = 11,ADC2								
ST	Initiate voltage comparison between ADC input Channel and SAD<7:0> value Note: Set by Software and reset by Hardware								
SAD<7:4>	Most Significant nibble of DAC input word								
SADB	0	0	0	DC COMP	SAD<3>	SAD<2>	SAD<1>	SAD<0>	00H
DC COMP	0 - DC Comparator mode disabled 1 - DC Comparator mode enabled								
SAD<3:0>	Least Significant nibble of 8 bit SAD value								
SP	SP<7>	SP<6>	SP<5>	SP<4>	SP<3>	SP<2>	SP<1>	SP<0>	07H
SP<7>	Stack Pointer								
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TF1	Timer 1 overflow Flag. Set by hardware on Timer/Counter overflow.Cleared by hardware when processor vectors to interrupt routine								
TR1	Timer 1 Run control bit. Set/Cleared by software to turn Timer/Counter on/off								
TF0	Timer 0 overflow Flag. Set by hardware on Timer/Counter overflow.Cleared by hardware when processor vectors to interrupt routine								
TR0	Timer 0 Run control bit. Set/Cleared by software to turn Timer/Counter on/off								
IE1	Interrupt 1 Edge flag (both edges generate flag). Set by hardware when external interrupt edge detected.Cleared by hardware when interrupt processed.								

Table 4 SFR Bit description

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
IT1	Interrupt 1 Type control bit. Set/Cleared by Software to specify edge/low level triggered external interrupts.								
IE0	Interrupt 0 Edge 1 flag. Set by hardware when external interrupt edge detected.Cleared by hardware when interrupt processed.								
IT0	Interrupt 0 Type flag.Set/Cleared by Software to specify falling edge/low level triggered external interrupts								
TDACH	TPWE	1	TD<13>	TD<12>	TD<11>	TD<10>	TD<9>	TD<8>	40H
TPWE	0 - Disable Tuning Pulse Width Modulator 1 - Enable Tuning Pulse Width Modulator								
TD<13:8>	Tuning Pulse Width Modulator High Byte								
TDACL	TD<7>	TD<6>	TD<5>	TD<4>	TD<3>	TD<2>	TD<1>	TD<0>	00H
TD<7:0>	Tuning Pulse Width Modulator Low Byte								
TH0	TH0<7>	TH0<6>	TH0<5>	TH0<4>	TH0<3>	TH0<2>	TH0<1>	TH0<0>	00H
TH0<7:0>	Timer 0 high byte								
TH1	TH1<7>	TH1<6>	TH1<5>	TH1<4>	TH1<3>	TH1<2>	TH1<1>	TH1<0>	00H
TH1<7:0>	Timer 1 high byte								
TL0	TL0<7>	TL0<6>	TL0<5>	TL0<4>	TL0<3>	TL0<2>	TL0<1>	TL0<0>	00H
TL0<7:0>	Timer 0 low byte								
TL1	TL1<7>	TL1<6>	TL1<5>	TL1<4>	TL1<3>	TL1<2>	TL1<1>	TL1<0>	00H
TL1<7:0>	Timer 1 low byte								
TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
Timer 1 Timer 0									
GATE	Gating Control Timer /Counter 1								
C/T	Counter (1) or Timer (0) selector								
M1,M0	Mode control bits M1,M0 = 00, 8 bit timer or 8 bit counter with divide by 32 prescaler M1,M0 = 01, 16 bit time interval or event counter M1,M0 = 10, 8 bit time interval or event counter with automatic reload upon overflow. Reload value stored in TH1 M1,M0 = 11, stopped								
GATE	Gating control Timer/Counter 0								
C/T	Counter (1) or Timer (0) selector								
M1,M0	Mode Control bits M1,M0 = 00, 8 bit timer or 8 bit counter with divide by 32 prescaler M1,M0 = 01, 16 bit time interval or event counter M1,M0 = 10, 8 bit time interval or event counter with automatic reload upon overflow. Reload value stored in TH0 M1,M0 = 11, one 8bit time interval or event counter and one 8bit time interval counter								
TXT0	X24 POSN	DISPLAY X24	-	DISABLE HEADER ROLL	DISPLAY STATUS ROW ONLY	-	VPS ON	INV ON	00H
X24 POSN	0 - Store X/24 in extension memory 1 - Store X/24 in basic page memory with packets 0 to 23								
DISLAY X24	0 - Display row 24 from basic page memory 1 - Display row 24 from appropriate location in extension memory								
DISABLE HEADER ROLL	0 - Write rolling headers and time to current display page 1 - Disable writing of rolling headers and time to into memory								

Table 4 SFR Bit description

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
DISPLAY STATUS ROW ONLY	0 - Display normal page rows 0 to 24 1 - Display only row 24								
VPS ON	0 - VPS acquisition off 1 - VPS acquisition on								
INV ON	0 - Inventory page off 1 - Inventory page on								
TXT1	EXT PKT OFF	8 BIT	ACQ OFF	X26 OFF	FULL FIELD	0	0	0	00H
EXT PKT OFF	0 - Acquire extension packets X/24,X/27,8/30/X 1 - Disable acquisition of extension packets								
8 BIT	0 - Error check and/or correct packets 0 to 24 1 - Disable checking of packets 0 to 24 written into memory								
ACQ OFF	0 - Write requested data into display memory 1 - Disable writing of data into Display memory								
X26 OFF	0 - Enable automatic processing of X/26 data 1 - Disable automatic processing of X/26 data								
FULL FIELD	0 - Acquire data only on VBI lines 1 - Acquire data on any TV line								
TXT2	(Reserved) 0	REQ<3>	REQ<2>	REQ<1>	REQ<0>	SC<2>	SC<1>	SC<0>	00H
REQ<3:0>	Page request								
SC<2:0>	Start column of page request								
TXT3				PRD<4>	PRD<3>	PRD<2>	PRD<1>	PRD<0>	00H
PRD<4:0>	Page Request data								
TXT4	OSD BANK ENABLE	QUAD WIDTH ENABLE	EAST/WEST	DISABLE DBL HEIGHT	B MESH ENABLE	C MESH ENABLE	TRANS ENABLE	SHADOW ENABLE	00H
OSD BANK ENABLE	0 - Only alpha numeric OSD characters available, 32 locations 1 - Alternate OSD location available via graphic attribute, additional 32 location								
QUAD WIDTH ENABLE	0 - Disable display of Quadruple width characters 1 - Enable display of Quadruple width characters								
EAST/WEST	0 - Western language selection of character codes A0 to FF 1 - Eastern character selection of character codes A0 to FF								
DISABLE DOUBLE HEIGHT	0 - Allow normal decoding of double height characters 1 - Disable normal decoding of double height characters								
B MESH ENABLE	0 - Normal display of black background 1 - Enable meshing of black background								
C MESH ENABLE	0 - normal display of coloured background 1 - Enable meshing of coloured background								
TRANS ENABLE	0 - Display black background as normal 1 - Display black background as video								
SHADOW ENABLE	0 - Disable display of shadow/fringing 1 - Display shadow/ fringe (default SE black)								
TXT5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN	03H
BKGND OUT	0 - Background colour not displayed outside teletext boxes 1 - Background colour displayed outside teletext boxes								

Table 4 SFR Bit description

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
BKGND IN	0 - Background colour not displayed inside teletext boxes 1 - Background colour displayed inside teletext boxes								
COR OUT	0 - COR not active outside teletext and OSD boxes 1 - COR active outside teletext and OSD boxes								
COR IN	0 - COR not active inside teletext and OSD boxes 1 - COR active inside teletext and OSD boxes								
TEXT OUT	0 - TEXT not displayed outside teletext boxes 1 - TEXT displayed outside teletext boxes								
TEXT IN	0 - TEXT not displayed inside teletext boxes 1 - TEXT displayed inside teletext boxes								
PICTURE ON OUT	0 - VIDEO not displayed outside teletext boxes 1 - VIDEO displayed outside teletext boxes								
PICTURE ON IN	0 - VIDEO not displayed inside teletext boxes 1 - VIDEO displayed inside teletext boxes								
TXT6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN	03H
BKGND OUT	0 - Background colour not displayed outside teletext boxes 1 - Background colour displayed outside teletext boxes								
BKGND IN	0 - Background colour not displayed inside teletext boxes 1 - Background colour displayed inside teletext boxes								
COR OUT	0 - COR not active outside teletext and OSD boxes 1 - COR active outside teletext and OSD boxes								
COR IN	0 - COR not active inside teletext and OSD boxes 1 - COR active inside teletext and OSD boxes								
TEXT OUT	0 - TEXT not displayed outside teletext boxes 1 - TEXT displayed outside teletext boxes								
TEXT IN	0 - TEXT not displayed inside teletext boxes 1 - TEXT displayed inside teletext boxes								
PICTURE ON OUT	0 - VIDEO not displayed outside teletext boxes 1 - VIDEO displayed outside teletext boxes								
PICTURE ON IN	0 - VIDEO not displayed inside teletext boxes 1 - VIDEO displayed inside teletext boxes								
TXT7	STATUS ROW TOP	CURSOR ON	REVEAL	BOTTOM/TOP	DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	00H
STATUS ROW TOP	0 - Display memory row 24 information below teletext page (on display row 24) 1 - Display memory row 24 information above teletext page (on display row 0)								
CURSOR ON	0 - Disable display of cursor 1 - Display cursor at position given by TXT9 and TXT10								
REVEAL	0 - Display as spaces characters in area with conceal attribute set 1 - Display characters in area with conceal attribute set								
BOTTOM/TOP	0 - Display memory rows 0 to 11 when double height bit is set 1 - Display memory rows 12 to 23 when double height bit is set								
DOUBLE HEIGHT	0 - Display each characters with normal height 1 - Display each character as twice normal height.								
BOX ON 24	0 - Disable display of teletext boxes in memory row 24 1 - Enable display of teletext boxes in memory row 24								
BOX ON 1-23	0 - Disable display of teletext boxes in memory row 1 to 23 1 - Enable display of teletext boxes in memory row 1 to 23								

Table 4 SFR Bit description

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
BOX ON 0	0 - Disable display of teletext boxes in memory row 0 1 - Enable display of teletext boxes in memory row 0								
TXT8	(Reserved) 0	FLICKER STOP ON	(Reserved) 0	DISABLE SPANISH	PKT 26 RECEIVED	WSS RECEIVED	WSS ON	0	00H
FLICKER STOP ON	0 - Enable 'Flicker Stopper' circuitry 1 - Disable 'Flicker Stopper' circuitry								
DISABLE SPANISH	0 - Enable special treatment of Spanish packet 26 characters 1 - Disable special treatment of Spanish packet 26 characters								
PKT 26 RECEIVED	0 - No packet 26 data has been processed 1 - Packet 26 data has been processed. Note: This flag is set by Hardware and must be reset by Software								
WSS RECEIVED	0 - No Wide Screen Signalling data has been processed 1 - Wide Screen signalling data has been processed Note: This flag is set by Hardware and must be reset by Software.								
WSS ON	0 - Disable acquisition of WSS data. 1 - Enable acquisition of WSS data.								
TXT9	CURSOR FREEZE	CLEAR MEMORY	A0	R<4>	R<3>	R<2>	R<1>	R<0>	00H
CURSOR FREEZE	0 - Use current TXT9 and TXT10 values for cursor position. 1 - Lock cursor at current position								
CLEAR MEMORY	0 - Clear memory block not requested 1 - Clear memory block pointed to by TXT15 Note: This flag is set by Software and reset by Hardware								
A0	0 - Access memory block pointed to by TXT15 1 - Access extension packet memory								
R<4:0>	Current memory ROW value. Note: Valid range TXT mode 0 to 24.								
TXT10	0	0	C<5>	C<4>	C<3>	C<2>	C<1>	C<0>	00H
C<5:0>	Current memory COLUMN value. Note: Valid range TXT mode 0 to 39.								
TXT11	D<7>	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>	00H
D<7:0>	Data value written or read from memory location defined by TXT9, TXT10 and TXT15								
TXT12	625/525 SYNC	Spanish	ROM VER<3>	ROM VER<2>	ROM VER<1>	ROM VER<0>	1	VIDEO SIGNAL QUALITY	xxxxxx1xB
625/525 SYNC	0 - 625 line CVBS signal is being received 1 - 525 line CVBS signal is being received								
Spanish	0 - Spanish character set not present in device 1 - Spanish character set present in device								
ROM VER<3:0>	Mask programmable identification for character set								
VIDEO SIGNAL QUALITY	0 - Acquisition can not be synchronised to CVBS input 1 - Acquisition can be synchronised to CVBS input								
TXT13	VPS RECEIVED	PAGE CLEARING	525 DISPLAY	525 TEXT	625 TEXT	PKT 8/30	FASTEXT	0	xxxxxxx0B
VPS RECEIVED	0 - VPS data not being received 1 - VPS data being received								
PAGE CLEARING	0 - No page clearing active 1 - Software or Power On page clear in progress								

Table 4 SFR Bit description

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
525 DISPLAY	0 - 625 Line synchronisation for Display 1 - 525 Line synchronisation for Display								
525 TEXT	0 - 525 Line WST not being received 1 - 525 line WST being received								
625 TEXT	0 - 625 Line WST not being received 1 - 625 line WST being received								
PKT 8/30	0 - No Packet 8/30/x(625) or Packet 4/30/x(525) data detected 1 - Packet 8/30/x(625) or Packet 4/30/x(525) data detected								
FASTEXT	0 - No Packet x/27 data detected 1 - Packet x/27 data detected								
TXT14	0	0	0	(Reserved) 0	PAGE<3>	PAGE<2>	PAGE<1>	PAGE<0>	00H
PAGE<3:0>	Current Display page								
TXT15	0	0	0	(Reserved) 0	BLOCK<3>	BLOCK<2>	BLOCK<1>	BLOCK<0>	00H
BLOCK<3:0>	Current Micro block to be accessed by TXT9, TXT10 and TXT11								
TXT17	0	FORCE ACQ<1>	FORCE ACQ<0>	FORCE DISP<1>	FORCE DISP<0>	SCREEN COL2	SCREEN COL1	SCREEN COL0	00H
FORCE ACQ<1:0>	00 - Automatic Selection 01 - Force 525 timing, Force 525 Teletext Standard 10 - Force 625 timing, Force 625 Teletext Standard 11 - Force 625 timing, Force 525 Teletext Standard								
FORCE DISP<1:0>	00 - Automatic Selection 01 - Force Display to 525 mode (9 lines per row) 10 - Force Display to 625 mode (10 lines per row) 11 - Not Valid (default to 625)								
SCREEN COL<2:0>	Defines colour to be displayed instead of TV picture and black background. The bits <2:0> are equivalent to the RGB components 000 - Transparent 001 - CLUT entry 9 010 - CLUT entry 10 011 - CLUT entry 11 100 - CLUT entry 12 101 - CLUT entry 13 110 - CLUT entry 14 111 - CLUT entry 15								
TXT18	NOT<3>	NOT<2>	NOT<1>	NOT<0>	0	0	BS<1>	BS<0>	00H
NOT<3:0>	National Option table selection, maximum of 32 when used with East/West bit								
BS<1:0>	Basic Character set selection								
TXT19	TEN	TC<2>	TC<1>	TC<0>	0	0	TS<1>	TS<0>	00H
TEN	0 - Disable Twist function 1 - Enable Twist character set								
TC<2:0>	Language control bits (C12/C13/C14) that has Twisted character set								
TS<1:0>	Twist Character set selection								
TXT20	DRCS ENABLE	OSD PLANES	0	0	OSD LANG ENABLE	OSD LAN<2>	OSD LAN<1>	OSD LAN<0>	00H
DRCS ENABLE	0 - Normal OSD characters used 1 - Re-map column 8 and 9 to DRCS.								
OSD PLANES	0 - Character code columns 8 and 9 defined as single plane characters (two colours per character). 1 - Character code columns 8 and 9 defined as two plane characters (four colours per character).								

Table 4 SFR Bit description

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
OSD LANG ENABLE	Enable use of OSD LAN<2:0> to define language option for display, instead of C12/C13/C14								
OSD LAN<2:0>	Alternative C12/C13/C14 bits for use with OSD menus								
TXT21	DISP LINES<1>	DISP LINES<0>	CHAR SIZE<1>	CHAR SIZE<0>	0	CC ON	I2C PORT0	CC/TXT	02H
DISP LINES<1:0>	The number of display lines per character row. 00 - 10 lines per character (defaults to 9 lines in 525 mode) 01 - 13 lines per character 10 - 16 lines per character 11 - reserved								
CHAR SIZE<1:0>	Character matrix size. 00 - 10 lines per character (matrix 12x10) 01 - 13 lines per character (matrix 12x13) 10 - 16lines per character (matrix 12x16) 11 - reserved								
CCON	0 - Closed Caption acquisition off 1 - Closed Caption acquisition on								
I2C PORT0	0 - disable I2C PORT0 1 - enable I2C PORT0 selection (P1.7/SDA0, P1.6/SCL0)								
CC/TXT	0 - Display configured for TXT mode 1 - Display configured for CC mode								
WDT	WDV<7>	WDV<6>	WDV<5>	WDV<4>	WDV<3>	WDV<2>	WDV<1>	WDV<0>	00H
WDV<7:0>	Watch Dog Timer period								
WDTKEY	WKEY<7>	WKEY<6>	WKEY<5>	WKEY<4>	WKEY<3>	WKEY<2>	WKEY<1>	WKEY<0>	00H
WKEY<7:0>	Watch Dog Timer Key Note: Must be set to 55H to disable Watch dog timer when active								
WSS1	0	0	0	WSS<3:0> ERROR	WSS<3>	WSS<2>	WSS<1>	WSS<0>	00H
WSS<3:0> ERROR	0 - No error in WSS<3:0> 1 - Error in WSS<3:0>								
WSS<3:0>	Signalling bits to define aspect ratio (group 1)								
WSS2	0	0	0	WSS<7:4> ERROR	WSS<7>	WSS<6>	WSS<5>	WSS<4>	00H
WSS<7:4> ERROR	0 - No errors in WSS<7:4> 1 - Error in WSS<7:4>								
WSS<7:4>	Signalling bits to define enhanced services (group 2)								
WSS3	WSS<13:11> ERROR	WSS<13>	WSS<12>	WSS<11>	WSS<10:8> ERROR	WSS<10>	WSS<9>	WSS<8>	00H
WSS<13:11> ERROR	0 - No error in WSS<13:11> 1 - Error in WSS<13:11>								
WSS<13:11>	Signalling bits to define reserved elements (group 4)								
WSS<10:8> ERROR	0 - No error in WSS<10:8> 1 - Error in WS<10:8>								
WSS<10:8>	Signalling bits to define subtitles (group 3)								
XRAMP	XRAMP<7>	XRAMP<6>	XRAMP<5>	XRAMP<4>	XRAMP<3>	XRAMP<2>	XRAMP<1>	XRAMP<0>	00H
XRAMP<7:0>	Internal RAM access upper byte address								

Table 4 SFR Bit description

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Character Set Feature Bits

Features available on the TDA935X/6X/8X devices are reflected in a specific area of the character ROM. These sections of the character ROM are mapped to two Special Function Registers: TXT22 and TXT12. Character ROM address 09FEH is mapped to SFR TXT22 as shown in Table 5. Character ROM address 09FFH is mapped to SFR TXT12 as shown in Table 7.

MAPPED ITEMS	11	10	9	8	7	6	5	4	3	2	1	0
Character ROM; address 09FEH	X	X	X	X	X	X	X	U	U	U	U	X
Mapped to TXT22	–	–	–	–	7	6	5	4	3	2	1	0
U = Used, X = Reserved												

Table 5 Character Rom - TXT22 mapping

BIT	FUNCTION
0	Reserved
1	1 = Text Acquisition available 0 = Text Acquisition not available
2	1 = Closed Caption Acquisition available 0 = Closed Caption Acquisition not available
3	1 = PWM0, PWM1, PWM2 and PWM3 not present 0 = PWM0, PWM1, PWM2 and PWM3 output on Port 3.0 to Port 3.3 respectively
4	1 = 10 page available 0 = 6 page available
5 to 11	Reserved

Table 6 Description of Character ROM address 09FEH bits

MAPPED ITEMS	11	10	9	8	7	6	5	4	3	2	1	0
Character ROM; address 09FFH	X	X	X	X	X	X	X	U	X	X	X	X
Mapped to TXT2	–	–	–	–	–	–	–	6	5	4	3	2
4 = Used, 5 = Reserved												

Table 7 Character Rom - TXT12 mapping

BIT	FUNCTION
4	1 = Spanish character set present 0 = no Spanish character set present
0 to 3, 5 to 11	Reserved

Table 8 Description of Character ROM address 0X 09FFH bits

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embedded μ -Controller

TDA 935X/6X/8X series

External (Auxiliary) Memory

The normal 80C51 external memory area has been mapped internally to the device, this means that the MOVX instruction accesses memory internal to the device.

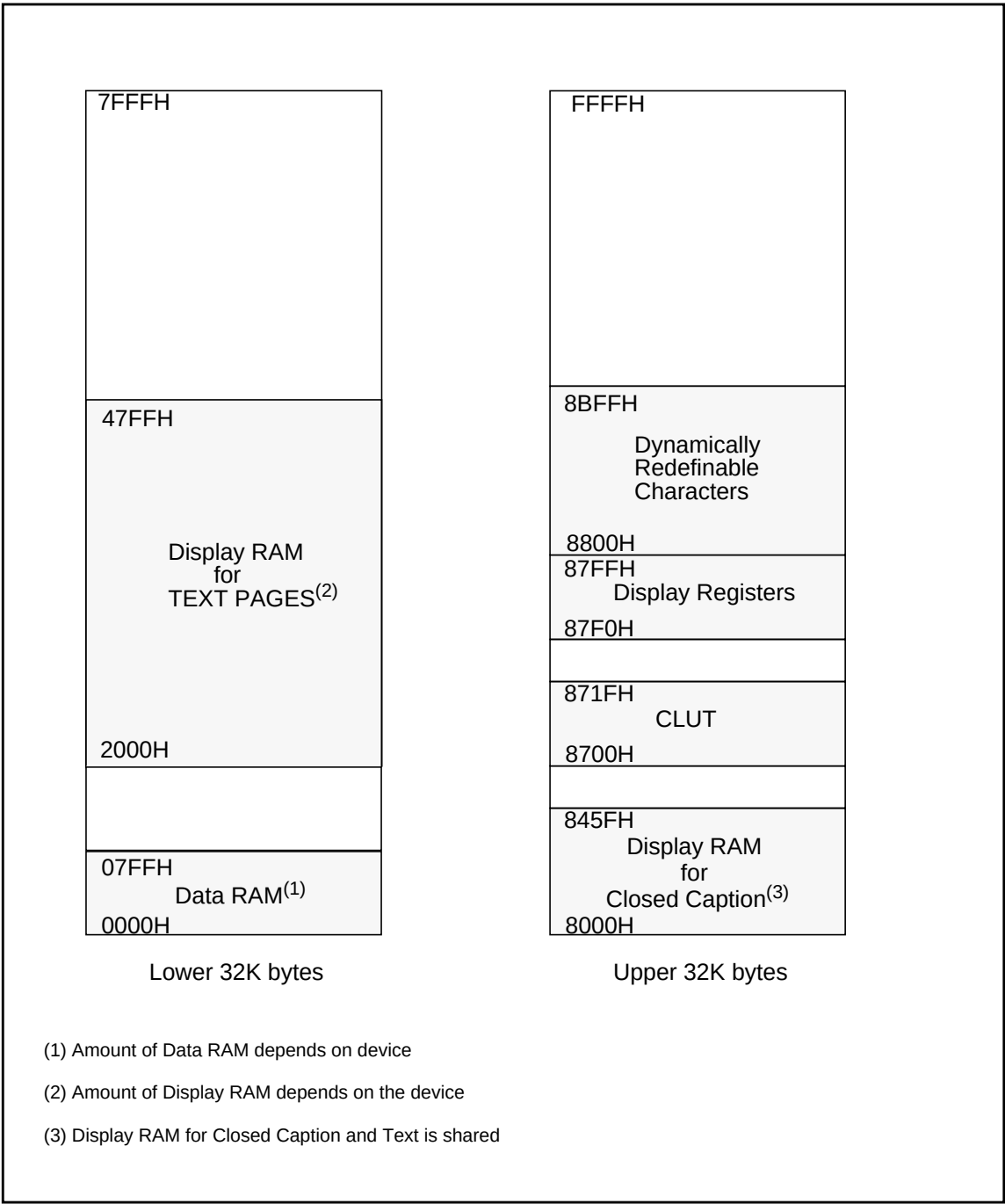


Figure 11 Auxiliary RAM allocation

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Auxiliary RAM Page Selection

The Auxiliary RAM page selector is used to select one of the 256 pages within the auxiliary RAM, not all pages are allocated, refer to Figure 11 for further detail. A page consists of 256 consecutive bytes.

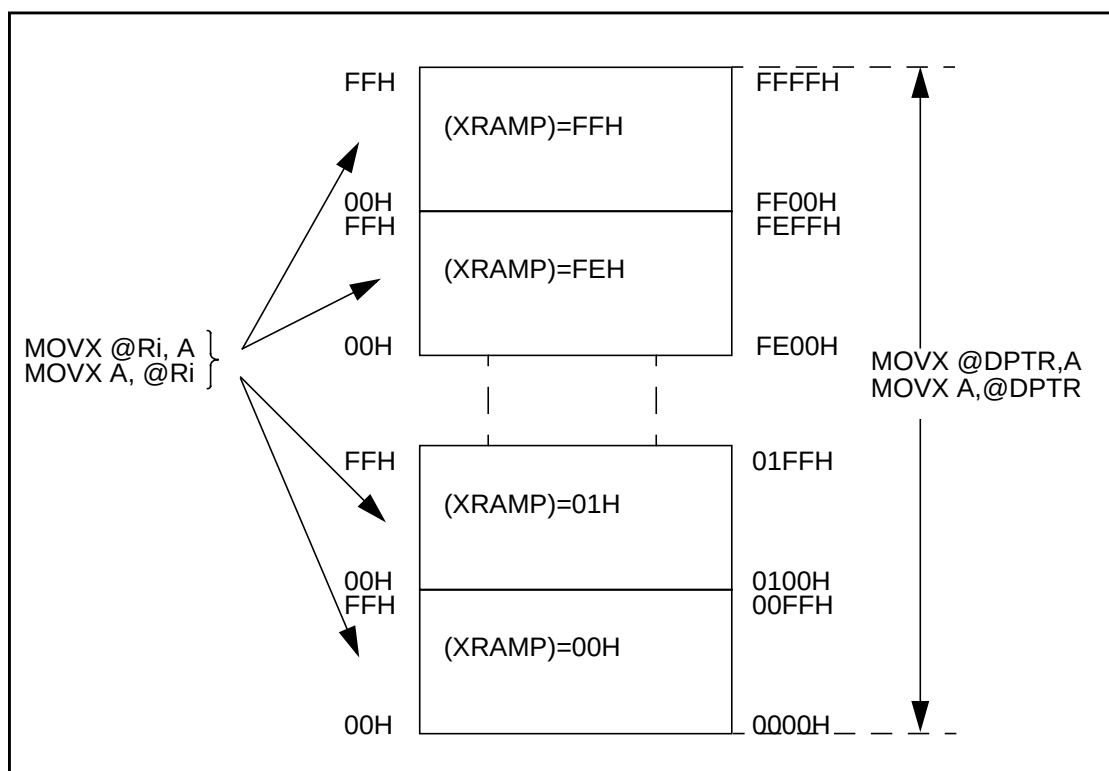


Figure 12 Indirect addressing of AUX-RAM

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Power-on Reset

An automatic reset can be obtained when VDD is applied by connecting the RESET pin to VDDP through a 10 μ F capacitor, providing the VDD rise time does not exceed 1ms, and the oscillator start-up time does not exceed 10ms.

To ensure correct initialisation, the RESET pin must be held high long enough for the oscillator to settle following power-up, usually a few milli-seconds. Once the oscillator is stable, a further 12 clocks are required to generate the Reset (One machine cycle of the Micro-controller). Once the above reset condition has been detected an internal reset signal is triggered which remains active for 2048 clock cycles.

Reduced Power modes

There are three power saving modes: Stand-by, Idle and Power Down. In all three modes the 3.3v power supplies (Vddp, Vddc & Vdda) to the device must be maintained. Power saving is achieved by clock gating on a section by section basis.

STAND-BY MODE

When Stand-by mode is entered both Acquisition and Display sections are disabled. The following functions remain active:-

- 80c51 Core
- Memory Interface
- I2C
- Timer/Counters
- WatchDog Timer
- Software A/D
- Pulse Width Modulators

To enter Stand-by mode, the STANDBY control bit in the ROMBANK SFR (Bit-7) must be set. It can be used in conjunction with either Idle or Power-Down to switch between power saving modes. This mode enables the 80c51 core to decode either IR Remote Commands or receive IIC commands without the need to fully power the device.

The Stand-by state is maintained upon exit from Idle / Power-Down. No wake-up from Stand-by is necessary as the 80c51 core remains operational.

Since the output values on RGB and VDS are maintained the teletext/OSD display must be disabled before entering this mode.

IDLE MODE

During Idle mode, Acquisition, Display and the CPU sections of the device are disabled. The following functions remain active:-

- Memory Interface
- I2C
- Timer/Counters

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- WatchDog Timer
- Pulse Width Modulators

To enter Idle mode the IDL bit in the PCON register must be set. The WatchDog timer must be disabled prior to entering Idle to prevent the device being reset. Once in Idle mode, the XTAL oscillator continues to run, but the internal clock to the CPU, Acquisition and Display are gated out. However, the clocks to the Memory Interface, I2C, Timer/Counters, WatchDog Timer and Pulse Width Modulators are maintained. The CPU state is frozen along with the status of all SFRs, internal RAM contents are maintained, as are the device output pin values. Since the output values on RGB and VDS are maintained the teletext/OSD display must be disabled before entering this mode.

There are three methods available to recover from Idle:-

- Assertion of an enabled interrupt will cause the IDL bit to be cleared by hardware, thus terminating Idle mode. The interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one after the instruction that put the device into Idle mode.
- A second method of exiting Idle is via an Interrupt generated by the SAD DC Compare circuit. When Painter is configured in this mode, detection of an analogue threshold at the input to the SAD may be used to trigger wake-up of the device i.e. TV Front Panel Key-press. As above, the interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one following the instruction that put the device into Idle. For further details of the SAD DC Compare mode refer to the Software A/D description within the micro-controller section.
- The third method of terminating Idle mode is with an external hardware reset. Since the oscillator is running, the hardware reset need only be active for one machine cycle (12 clocks at 12MHz) to complete the reset operation. Reset defines all SFRs and Display memory to a pre-defined state, but maintains all other RAM values. Code execution commences with the Program Counter set to '0000'.

POWER DOWN MODE

In Power Down mode the XTAL oscillator is stopped. The contents of all SFR, and RAM is maintained, however the Auxiliary/Display memory is not maintained. The port pins maintain the values defined by the SFR's. Since the output values on RGB and VDS are maintained the teletext/OSD display must be made inoperative before entering Power Down mode.

The power down mode is activated by setting the PD bit in the PCON register. The WatchDog timer must be disabled before entering Power down.

There are two methods of exiting power down. Since the clock is stopped, external interrupts needs to be set to level sensitive, by changing the level of these interrupts the device can be taken out of power down.

The second method of terminating the power down mode is with an external hardware reset. Reset defines all SFR's and Display memory, but maintains all other RAM values.

I/O Facility

I/O PORTS

The device has a number of micro-controller port I/O lines, each are individually addressable.

The I²C-bus ports (P1.6 and P1.7) can only be configured as Open-drain.

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PORT TYPE

All individual ports bits can be programmed to function in one of four modes, the mode is defined by eight Port Configuration SFR's (P0CFGA/P0CFGB, P1CFGA/P1CFGB, P2CFGA/P2CFGB and P3CFGA/P3CFGB). The modes available are Open Drain, Quasi-bidirectional, High Impedance, Push-Pull.

Open Drain

The Open drain mode can be used for bi-directional operation of a port. It requires an external pull-up resistor, the pull-up voltage has a maximum value of 5.5V, to allow connection of the device into a 5V environment.

Quasi-bidirectional

The quasi-bidirectional mode is a combination of open drain and push pull. It requires an external pull-up resistor to VDDp (nominally 3.3V). When a signal transition from 0 to 1 is output from the device, the pad is put into push-pull mode for one clock cycle (166ns) after which the pad goes into open drain mode. The mode may be used to speed up the edges of signal transitions. This is the default mode of operation of the pads after reset.

High Impedance

The high impedance mode can be used for Input only operation of the port. When using this configuration the two output transistors are turned off.

Push-Pull

The push pull mode can be used for output only. In this mode the signal is driven to either 0V or VDDp, which is nominally 3.3V.

Interrupt System

The device has 7 interrupt sources, each of which can be enabled or disabled. When enabled each interrupt can be assigned one of two priority levels. There are four interrupts that are common to the 80C51, two of these are external interrupts (EX0 and EX1) and the other two are timer interrupts (ET0 and ET1). In addition to the conventional 80c51, two application specific interrupts are incorporated internal to the device which have following functionality:-

ECC (Closed Caption Data Ready Interrupt) - This interrupt is generated when the device is configured in Closed Caption Acquisition mode. The interrupt is activated at the end of the currently selected Slice Line as defined in the CCLIN SFR.

EBUSY (Display Busy Interrupt) - An interrupt is generated when the Display enters either a Horizontal or Vertical Blanking Period. i.e. Indicates when the micro-controller can update the Display RAM without causing undesired effects on the screen. This interrupt can be configured in one of two modes using the MMR Configuration Register (Address 87FF, Bit-3 [TXT/V]):-

- **TeXT Display Busy:** An interrupt is generated on each active horizontal display line when the Horizontal Blanking Period is entered.
- **Vertical Display Busy:** An interrupt is generated on each vertical display field when the Vertical Blanking Period is entered.

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Interrupt Enable Structure

Each of the individual interrupt can be enable or disable by setting or clearing the relevant bit in the interrupt enable SFR called IE. All interrupt sources can also be globally disabled by clearing the EA bit (IE.7)

The interrupt structure is shown in Figure 13.

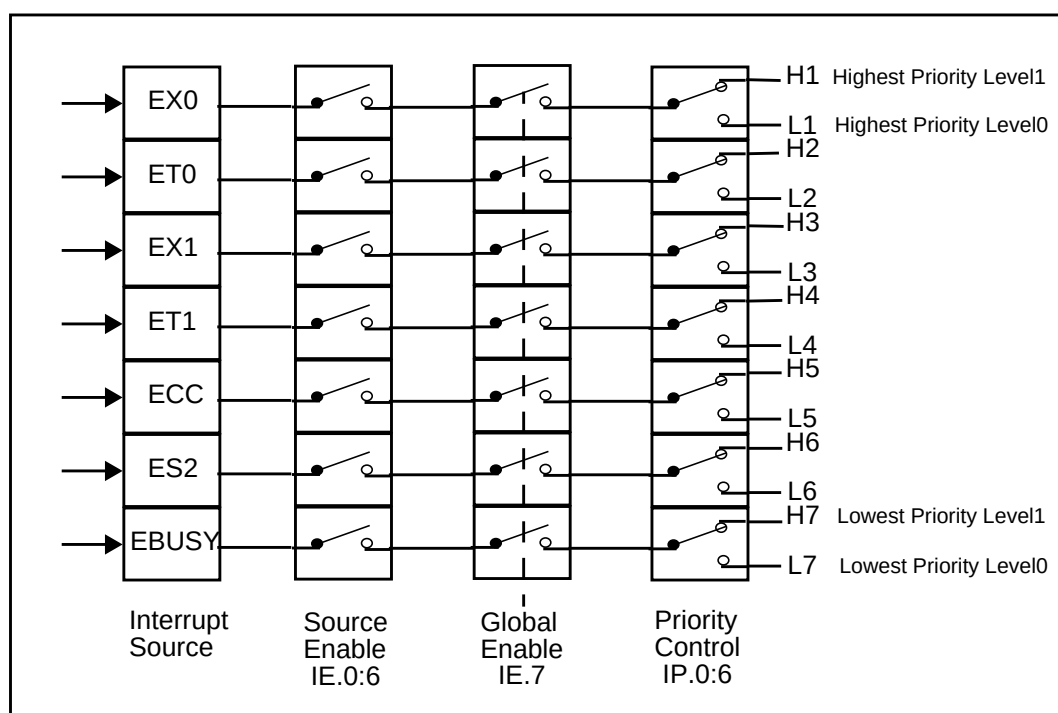


Figure 13 Interrupt Structure

Interrupt Enable Priority

Each interrupt source can be assigned one of two priority levels. The interrupt priority are defined by the interrupt priority SFR called IP. A low priority interrupt can be interrupted by a high priority interrupt, but not by another low priority interrupt. A high priority interrupt can not be interrupted by any other interrupt source. If two requests of different priority level are received simultaneously, the request with the highest priority level is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus, within each priority level there is a second priority structure determined by the polling sequence as defined in Table 9

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Source	Priority within level	Interrupt Vector
EX0	Highest	0003H
ET0	-	000BH
EX1	-	0013H
ET1	-	001BH
ECC	-	0023H
ES2	-	002BH
EBUSY	Lowest	0033H

Table 9 Interrupt Priority (within same level)INTERRUPT VECTOR ADDRESS

The processor acknowledges an interrupt request by executing a hardware generated LCALL to the appropriate servicing routine. The interrupt vector addresses for each source are shown in Table 9.

LEVEL/EDGE INTERRUPT

The external interrupt can be programmed to be either level-activated or transition activated by setting or clearing the IT0/1 bits in the Timer Control SFR called TCON.

ITx	Level	Edge
0	Active low	
1		INT0 = Negative Edge INT1 = Positive and Negative Edge

Table 10 External Interrupt Activation

The external interrupt INT1 differs from the standard 80C51 in that it is activated on both edges when in edge sensitive mode. This is to allow software pulse width measurement for handling remote control inputs.

Timer/Counter

Two 16 bit timers/counters are incorporated Timer0 and Timer1. Both can be configured to operate as either timers or event counters.

In Timer mode, the register is incremented on every machine cycle. It is therefore counting machine cycles. Since the machine cycle consists of 12 oscillator periods, the count rate is $1/12 F_{osc} = 1\text{MHz}$.

In Counter mode, the register is incremented in response to a negative transition at its corresponding external pin T0 or T1. Since the pins T0 and T1 are sampled once per machine cycle it takes two machine cycles to recognise a transition, this gives a maximum count rate of $1/24 F_{osc} = 0.5\text{MHz}$.

There are six special function registers used to control the timers/counters. These are:

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TCON, TMOD, TL0, TH0, TL1 and TH1.

The Timer/Counter function is selected by control bits C/T in the Timer Mode SFR(TMOD). These two Timer/Counter have four operating modes, which are selected by bit-pairs (M1.M0) in the TMOD. Details of the modes of operation are given in the "80C51 Based 8-Bit Microcontrollers - Philips Semiconductors (ref. IC20)" (Reference [1]).

TL0 and TH0 are the actual timer/counter registers for timer 0. TL0 is the low byte and TH0 is the high byte. TL1 and TH1 are the actual timer/counter registers for timer 1. TL1 is the low byte and TH1 is the high byte.

WatchDog Timer

The WatchDog timer is a counter that when it overflows forces the microcontroller in to a reset. The purpose of the WatchDog timer is to reset the microcontroller if it enters an erroneous processor state (possibly caused by electrical noise or RFI) within a reasonable period of time. When enabled, the WatchDog circuitry will generate a system reset if the user program fails to reload the WatchDog timer within a specified length of time known as the WatchDog interval.

The WatchDog timer consists of an 8-bit counter with an 11 bit prescaler. The prescaler is fed with a signal whose frequency is $1/12 f_{osc}$ (1MHz). The 8 bit timer is incremented every 't' seconds where:

$$t = 12 \times 2048 \times 1 / f_{osc} = 12 \times 2048 \times 1 / 12 \times 10^6 = 2.048 \text{ms}$$

WATCHDOG TIMER OPERATION

The WatchDog operation is activated when the WLE bit in the Power Control SFR (PCON) is set. The WatchDog can be disabled by Software by loading the value 55H into the WatchDog Key SFR (WDTKEY). This must be performed before entering Idle/Power Down mode to prevent exiting the mode prematurely.

Once activated the WatchDog timer SFR (WDT) must be reloaded before the timer overflows. The WLE bit must be set to enable loading of the WDT SFR, once loaded the WLE bit is reset by hardware, this is to prevent erroneous Software from loading the WDT SFR.

The value loaded into the WDT defines the WatchDog interval.

$$\text{WatchDog interval} = (256 - \text{WDT}) * t = (256 - \text{WDT}) * 2.048 \text{ms}$$

The range of intervals is from WDT = 00H which gives 524ms to WDT = FFH which gives 2.048ms

PORT Alternate Functions

The Ports 1,2 and 3 are shared with alternate functions to enable control of external devices and circuitry. The alternate functions are enabled by setting the appropriate SFR and also writing a logic '1' to the Port bit that the function occupies.

If the Pulse Width Modulator outputs (PWM) are required on Ports 3.0 to 3.3, they require an additional bit to be set in the Character ROM. If this facility is required, it should be requested when ordering the Language Set.

The PWMs may be enabled per pin, thus giving any combination of either PWM output, SFR output or SAD input.

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PWM PULSE WIDTH MODULATORS

The device has up to 4 6-bit Pulse Width Modulated (PWM) outputs for analogue control of e.g. volume, balance, bass, treble, brightness, contrast, hue and saturation. The PWM outputs generate pulse patterns with a repetition rate of 21.33us, with the high time equal to the PWM SFR value multiplied by 0.33us. The analogue value is determined by the ratio of the high time to the repetition time, a D.C. voltage proportional to the PWM setting is obtained by means of an external integration network (low pass filter).

PWM Control

The relevant PWM is enabled by setting the PWM enable bit PWxE in the PWMx Control register. The high time is defined by the value PWxV<5:0>

TPWM TUNING PULSE WIDTH MODULATOR

The device has a single 14-bit PWM that can be used for Voltage Synthesis Tuning. The method of operation is similar to the normal PWM except the repetition period is 42.66us.

TPWM Control

Two SFR are used to control the TPWM, they are TDACL and TDACH. The TPWM is enabled by setting the TPWE bit in the TDACH SFR. The most significant bits TD<13:7> alter the high period between 0 and 42.33us. The 7 least significant bits TD<6:0> extend certain pulses by a further 0.33us. e.g. if TD<6:0> = 01H then 1 in 128 periods will be extended by 0.33us, if TD<6:0>=02H the 2 in 128 periods will be extended.

The TPWM will not start to output a new value until writing a value to TDACH. Therefore, if the value is to be changed TACL should be written before TDACH.

SAD SOFTWARE A/D

Four successive approximation Analogue to Digital Converters can be implemented in software by making use of the on board 8-bit Digital to Analogue Converter and Analogue Comparator.

SAD Control

The control of the required analogue input is done using the channel select bits CH<1:0> in the SAD SFR, this selects the required analogue input to be passed to one of the inputs of the comparator. The second comparator input is generated by the DAC whose value is set by the bits SAD<7:0> in the SAD and SADB SFR's. A comparison between the two inputs is made when the start compare bit ST in the SAD SFR is set, this must be at least one instruction cycle after the SAD<7:0> value has been set. The result of the comparison is given on VHI one instruction cycle after the setting of ST

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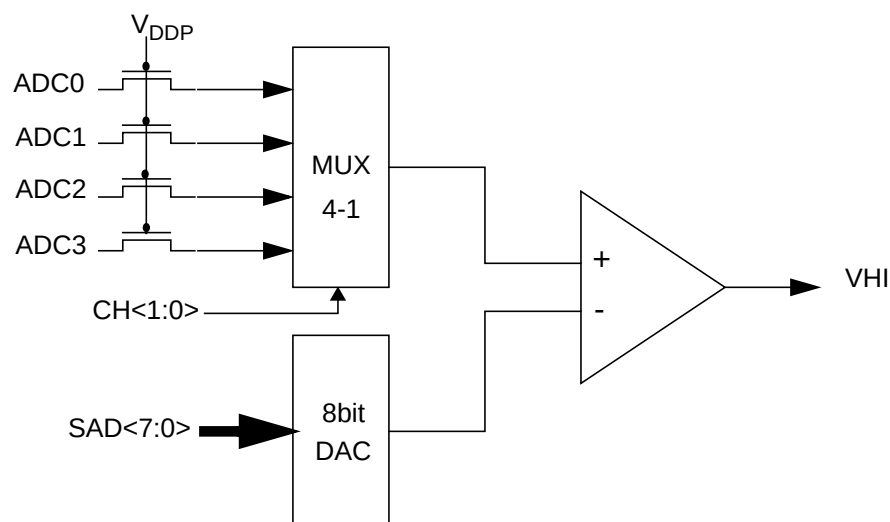


Figure 14 SAD Block Diagram

SAD Input Voltage

The external analogue voltage that is used for comparison with the internally generated DAC voltage do not have the same voltage range. The DAC has a lower reference level of V_{SSA} and an upper reference level of V_{SSA} . The resolution of the DAC voltage with a nominal values is $3.3/256 \sim 13\text{mv}$. The external analogue voltage has a lower value equivalent to V_{SSA} and an upper value equivalent to $V_{DDP} - V_{tn}$, where V_{tn} is the threshold voltage for an NMOS transistor. The reason for this is that the input pins for the analogue signals (P3.0 to P3.3) are 5V tolerant for normal port operations, i.e. when not used as analogue input. To protect the analogue multiplexer and comparator circuitry from the 5V, a series transistor is used to limit the voltage. This limiting introduces a voltage drop equivalent to V_{tn} ($\sim 0.6\text{V}$) on the input voltage. Therefore for an input voltage in the range V_{DDP} to $V_{DDP} - V_{tn}$ the SAD returns the same comparison value.

When utilising Port 3.0 to Port 3.3 for SAD operation, the associated PWM outputs must be disabled.

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SAD DC Comparator mode

The SAD module incorporates a DC Comparator mode which is selected using the 'DC_COMP' control bit in the SADB SFR. This mode enables the microcontroller to detect a threshold crossing at the input to the selected analog input pin (P3.0/ADC0, P3.1/ADC1, P3.2/ADC2 or P3.3/ADC3) of the software ADC. A level sensitive interrupt is generated when the analog input voltage level at the pin falls below the analog output level of the SAD Digital-to-Analog Converter.

This mode is intended to provide the device with a wake-up mechanism from Power-down or Idle mode when a key-press on the front panel of the TV is detected.

The following software sequence should be used when utilizing this mode for Power-down or Idle mode:

1. Disable INT1 using the IE SFR
2. Set INT1 to level sensitive using the TCON SFR
3. Set the DAC digital input level to the desired threshold level using SAD/SADB SFRs and select the required input pin (P3.0, P3.1, P3.2 or P3.3) using CH1 and CH0 in the SAD SFR
4. Enter DC Compare mode by setting the 'DC_COMP' enable bit in the SADB SFR
5. Enable INT1 using the IE SFR
6. Enter Power-down/Idle mode. Upon wake-up the SAD should be restored to its conventional operating mode by disabling the 'DC_COMP' control bit.

I²C Serial I/O Bus

The I²C bus consists of a serial data line (SDA on Port P1.7) and a serial clock line (SCL on Port P1.6).

These Ports may be enabled/disabled using TXT21.0 (I²C Port Enable Bit).

Within the device, two separate hardware modules utilise this Bus: The Micro-controller and the TV Signal Processor. The Micro-controller I²C peripheral may operate in four different configurations:

- Master Transmitter
- Master Receiver
- Slave Transmitter
- Slave Receiver

The TV Signal Processor may be addressed in Slave Mode only, either via the 80C51 micro-controller or from Port P1.6 and Port P1.7 by another master in the system.

I²C-bus control of the TV signal processor

For compatibility and possible re-use of software blocks, the I²C-bus control for the TV signal processor is organised as in the stand-alone TV signal processors. The internal communication is independent of the programming of the Ports P1.6 and P1.7. All details on the control of the TV signal processor are given in the description of the TV signal processor.

The byte level I²C serial port on the device is identical in operation/configuration to the I²C serial port on the 8xC558, with the exception of the clock rate selection bits CR<2:0>. The operation of the I²C subsystem is described in detail in the 8xC558 datasheet contained in reference [1].

TV signal processor-Teletext decoder with embedded μ -Controller

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I2C Port Selection

The selection of the SCL0/SDA0 port is done using TXT21.I2C PORT0 bit. When the port is enabled any information transmitted from the device goes onto the enabled port. Any information transmitted to the device can only be acted on if the port is enabled.

LED Support

Port pins P0.5 and P0.6 have an 8mA current sinking capability to enable LEDs in series with current limiting resistors to be driven directly, without the need for additional buffering circuitry.

Memory Interface

The memory interface controls access to the embedded DRAM, refreshing of the DRAM and page clearing. The DRAM is shared between Data Capture, Display and Microcontroller sections. The Data Capture section uses the DRAM to store acquired information that has been requested. The Display reads from the DRAM information and converts it into RGB values. The Microcontroller uses the DRAM as embedded auxiliary RAM and to generate OSD.

Memory Structure

The memory is partitioned into two distinct areas, the dedicated auxiliary RAM area, and the Display RAM area. The Display RAM area when not being used for Data Capture or Display can be used as an extension to the auxiliary RAM area.

AUXILIARY RAM

The auxiliary RAM is not initialised at power up. The contents of the auxiliary RAM are maintained during Idle mode, but are lost if Power Down mode is entered.

DISPLAY RAM

The Display RAM is initialised on power up to a value 20H. The contents of the Display RAM are maintained when entering Idle mode. If Idle mode is exited using an Interrupt then the contents are unchanged, if Idle mode is exited using a RESET then the Display RAM is initialised to 20H.

The size of the DRAM can be any value up to 2K.

Memory Mapping

The dedicated auxiliary RAM area occupies a maximum of 2K, with an address range from 0000H to 07FFH. The Display RAM occupies a maximum of 10K with an address range from 2000H to 47FFH for TXT mode and 8000H to 86FFH for CC mode (see Figure 15). The two modes although having different address ranges occupy physical the same DRAM area.

When not utilising the display memory, up to 12K is available for use as dedicated auxiliary RAM.

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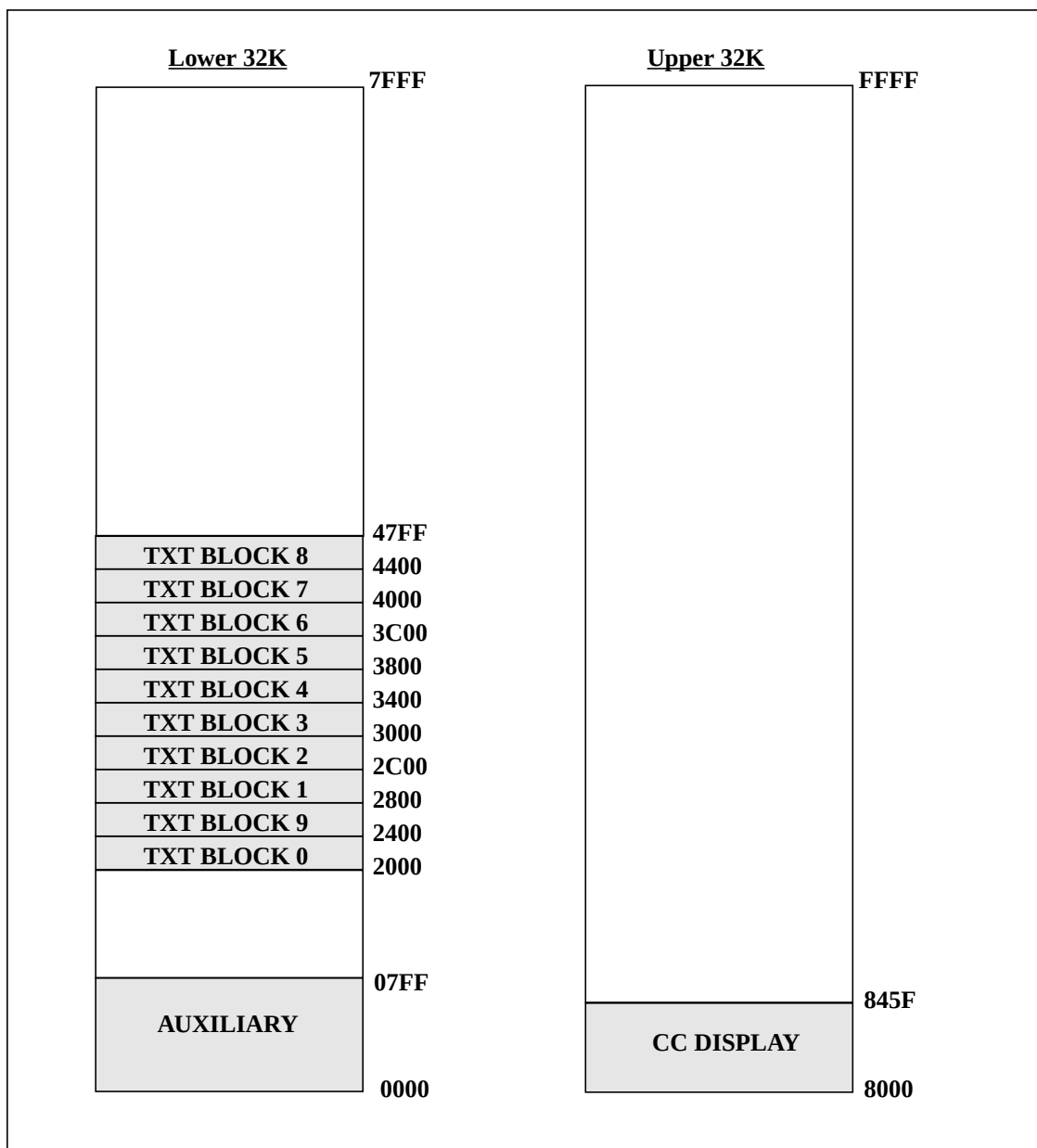


Figure 15 DRAM Memory mapping

Addressing Memory

The memory can be addressed by the Microcontroller in two ways, either directly using a MOVX command, or via Special Function Registers depending on what address is required.

The dedicated auxiliary RAM, and Display Memory in the range 8000H to 86FFH, can only be accessed using the MOVX command. The Display memory in the range 2000H to 47FFH can either be directly accessed using the MOVX, or via the Special Function Registers.

TV signal processor-Teletext decoder with embedded μ -Controller

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TXT DISPLAY MEMORY SFR ACCESS

The Display memory when in TXT mode is configured as 40 Columns wide by 25 Rows and occupies 1K x 8bits of memory (see Figure 16). There can be a maximum of 10 display pages. Using TXT15:Block<3:0> and TXT15:Micro Bank, the required display page can be selected to be written to. The row and column within that block is selected using TXT9:R<4:0> and TXT10:C<5:0>. The data at the selected position can either be written or read from by either writing to or reading from TXT11:D<7:0>.

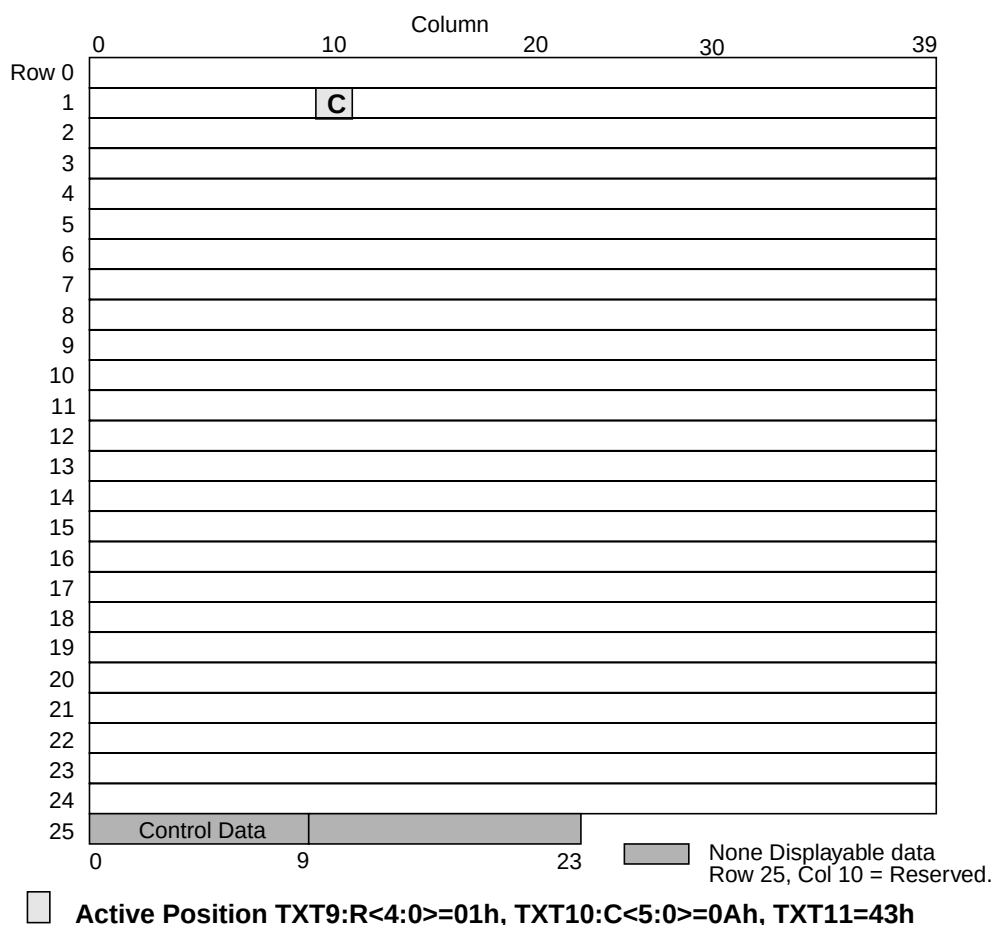


Figure 16 TXT Memory Map

When ever a read or write is performed on TXT11, the row values stored in TXT9 and column value stored in TXT10 are automatically incremented. For rows 0 to 24 the column value is incremented upto a maximum of 39, at which point it resets to 0 and increments the row counter value. When row 25 column 23 is reached the values of the row and column are both reset to 0.

Writing values outside of the valid range for TXT9 or TXT10 will cause undetermined operation of the auto-incrementing function for accesses to TXT11.

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TXT DISPLAY MEMORY MOVX ACCESS

It is important for the generation of OSD displays, that use this mode of access, to understand the mapping of the MOVX address onto the display row and column value. This mapping of row and column onto address is shown in Table 11. The values shown are added onto a base address for the required memory block (see Figure 15) to give a 16-bit address-

'Movx' Addresses shown in Hex.	Col. 0		Col. 23		Col. 31	Col. 32		Col. 39
Row 0	000		017		01F	3F8		3FF
Row 1	020		037		03F	3F0		3F7
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
Row 23	2E0		3F7		2FF	340		347
Row 24	300		317		31F	338		33F
Row 25	320		337					

Table 11 Column and Row to 'Movx' Address (Lower 10 bits of Address)

Page Clearing

Page Clearing is performed on request from either the Data Capture block, or the Microcontroller under the control of the embedded software.

At power on and reset the whole of the page memory is cleared. The TXT13.PAGE CLEARING bit will be set while this takes place.

DATA CAPTURE PAGE CLEAR

When a page header is acquired for the first time after a new page request or a page header is acquired with the erase (C4) bit set the page memory is 'cleared' to spaces before the rest of the page arrives.

When this occurs, the space code (20h) is written into every location of rows 1 to 23 of the basic page memory, the appropriate packet 27 row of the extension packet memory and the row where teletext packet 24 is written. This last row is either row 24 of the basic page memory, if the TXT0.X24 POSN bit is set, or the relevant row of the extension packet memory, if the bit is not set. Page clearing takes place before the end of the TV line in which the header arrived which initiated the page clear. This means that the 1 field gap between the page header and the rest of the page which is necessary for many teletext decoders is not required.

SOFTWARE PAGE CLEAR

The software can also initiate a page clear, by setting the TXT9.CLEAR MEMORY bit. When it does so, every location in the memory block pointed to by TXT15.BLOCK<3:0> is cleared. The CLEAR MEMORY bit is not latched so the software does not have to reset it after it has been set.

Only one page can be cleared in a TV line, so if the software requests a page clear it will be carried out on the next TV line on which the Data Capture hardware does not force the page to be cleared. A flag, TXT13.PAGE CLEARING, is provided to indicate that a software requested page clear is being carried out. The flag is set when a logic '1' is written into the TXT9.CLEAR MEMORY bit and is reset when the page clear has been completed.

**TV signal processor-Teletext decoder with
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TDA 935X/6X/8X series**Data Capture**

The Data Capture section takes in the analogue Composite Video and Blanking Signal (CVBS), and from this extracts the required data, which is then decoded and stored in memory.

The extraction of the data is performed in the digital domain. The first stage is to convert the analogue CVBS signal into a digital form. This is done using an ADC sampling at 12MHz. The data and clock recovery is then performed by a Multi-Rate Video Input Processor(MulVIP). From the recovered data and clock the following data types are extracted WST Teletext(625/525),Closed Caption, VPS, WSS. The extracted data is stored in either memory (DRAM) via the Memory Interface or in SFR locations.

Data Capture Features

- Video Signal Quality detector
- Data Capture for 625 line WST
- Data Capture for 525 line WST
- Data Capture for US Closed Caption
- Data Capture for VPS data (PDC system A)
- Data Capture for Wide Screen Signalling (WSS) bit decoding
- Automatic selection between 525 WST/625WST
- Automatic selection between 625WST/VPS on line 16 of VBI
- Real-time capture and decoding for WST Teletext in Hardware, to enable optimised microprocessor throughput
- Up to 10 pages stored On-Chip
- Inventory of transmitted Teletext pages stored in the Transmitted Page Table (TPT) and Subtitle Page Table (SPT)
- Automatic detection of FASTEXT transmission
- Real-time packet 26 engine in Hardware for processing accented, G2 and G3 characters
- Signal quality detector for WST/VPS data types
- Comprehensive Teletext language coverage
- Full Field and Vertical Blanking Interval (VBI) data capture of WST data

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Block Diagram for Data Capture

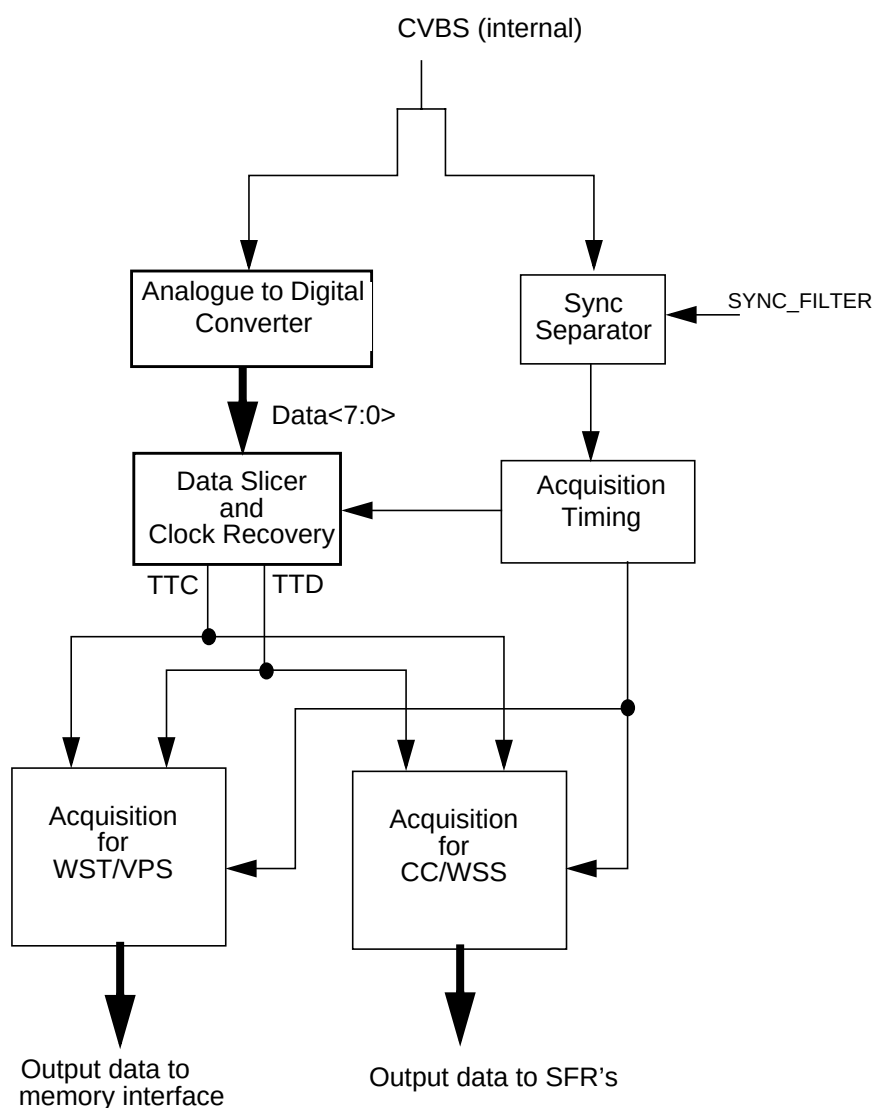


Figure 17 Data Capture Block Diagram

Analogue to Digital Converter

The output of the CVBS switch is passed to a differential to single ended converter (DIVIS), although in this device it is used as a single value and reference. The analogue output of DIVIS is converted into a digital representation by a full flash ADC with a sampling rate of 12MHz.

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Multi Rate Video Input Processor

The multi rate video input processor is a Digital Signal Processor designed to extract the data in serial form and recover the clock from a digitised CVBS signal.

DATA STANDARDS

The data and clock standards that can be recovered are shown in Table 12.

Data Standard	Clock Rate
625WST	6.9375 MHz
525WST	5.7272MHz
VPS	5.0MHz
WSS	5.0MHz
Closed Caption	500KHz

Table 12 Data Slicing Standards

Data Capture Timing

The Data Capture timing section uses the Synchronisation information extracted from the CVBS signal to generate the required Horizontal and Vertical reference timings.

The timing section automatically recognises and selects the appropriate timings for either 625 (50Hz) synchronisation or 525 (60Hz) synchronisation. A flag TXT12.Video Signal Quality is set when the timing section is locked correctly to the incoming CVBS signal. When TXT12.Video Signal Quality is set another flag TXT12.625/525 SYNC can be used to identify the standard.

Acquisition

The acquisition sections extracts the relevant information from the serial data stream received from the MuVIP section and writes it in to display memory.

WST ACQUISITION

The device is capable of acquiring level 1.5 625 Line and 525 Line World System Teletext (see Reference [3] and Reference [4]).

BROADCAST SERVICE DATA DETECTION

When a packet 8/30 is detected, or a packet 4/30 when the device is receiving a 525 line transmission, the TXT13. Pkt 8/30 flag is set. The flag can be reset by writing a logic 0 into the SFR bit.

FASTTEXT DETECTION

When a packet 27, designation code 0 is detected, whether or not it is acquired, the TXT13. FASTTEXT bit is set. If the device is receiving 525 line teletext, a packet X/0/27/0 is required to set the flag. The flag can be reset by writing a logic 0 into the SFR bit.

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VPS ACQUISITION

When the TXT0. VPS ON bit is set, any VPS data present on line 16, field 0 of the CVBS signal at the input of the teletext decoder is error checked and stored. The device automatically detects whether teletext or VPS is being transmitted on this line and decodes the data appropriately

	column																						
	0	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23							
row 25	Teletext page header data	VPS byte 11	VPS byte 12	VPS byte 13	VPS byte 14	VPS byte 15	VPS byte 4	VPS byte 5															

Figure 18 VPS Data Storage

Each VPS byte in the memory consists of 4 biphasic decoded data bits (bits 0-3), a biphasic error flag (bit 4) and three 0s (bits 5-7).

The TXT13. VPS Received bit is set by the hardware whenever VPS data is acquired. The flag can be reset by writing a logic 0 into the SFR bit.

Full details of the VPS system can be found in Reference [5].

WSS ACQUISITION

The Wide Screen Signalling data transmitted on line 23 gives information on the aspect ratio and display position of the transmitted picture, the position of subtitles and on the camera/film mode. Some additional bits are reserved for future use. A total of 14 data bits are transmitted.

All of the available data bits transmitted by the Wide Screen Signalling signal are captured and stored in SFR's WSS1, WSS2 and WSS3. The bits are stored as groups of related bits and an error flag is provided for each group to indicate when a transmission error has been detected in one or more of the bits in the group.

Wide screen signalling data is only acquired when the TXT8.WSS ON bit is set.

The TXT8.WSS RECEIVED bit is set by the hardware whenever wide screen signalling data is acquired. The flag can be reset by writing a logic 0 into the SFR bit.

CLOSED CAPTION ACQUISITION

The US Closed Caption data is transmitted on line 21 (525 line timings) and is used for Captioning information, Text information and Extended Data Services. Full Details can be found in Reference [6].

Closed Caption data is only acquired when TXT21.CC ON bit is set

Two bytes of data are stored per field in SFR's, the first byte is stored in CCDAT1 and the second byte is stored in CCDAT2. The value in the CCDAT registers are reset to 00h at the start of the Closed Caption line defined by CCLIN.CS<4:0>. At the end of the Closed Caption line an interrupt is generated if IE.ECC is active.

The processing of the Closed Caption data to convert into a displayable format is performed by the embedded Software.

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MAKING A PAGE REQUEST

A page is requested by writing a series of bytes into the TXT3.PRD<4:0> SFR which corresponds to the number of the page required. The bytes written into TXT3 are stored in a RAM with an auto-incrementing address. The start address for the RAM is set using the TXT2.SC<2:0> to define which part of the page request is being written, and TXT2.REQ<3:0> is used to define which of the 10 page requests is being modified. If TXT2.REQ<3:0> is greater than 09H, then data being written to TXT3 is ignored. Table 13 shows the contents of the page request RAM.

Up to 10 pages of teletext can be acquired on the 10 page device, when TXT1.EXT PKT OFF is set to logic 1, and up to 9 pages can be acquired when this bit is set to logic 0.

If the 'Do Care' bit for part of the page number is set logic 0 then that part of the page number is ignored when the teletext decoder is deciding whether a page being received off air should be stored or not. For example, if the Do Care bits for the four subcode digits are all set to logic 0 then every subcode version of the page will be captured. When the HOLD bit is set to a logic 0 the teletext decoder will not recognise any page as having the correct page number and no pages will be captured. In addition to providing the user requested hold function, this bit should be used to prevent the inadvertent capture of an unwanted page when a new page request is being made. For example, if the previous page request was for page 100 and this was being changed to page 234, it would be possible to capture page 200 if this arrived after only the requested magazine number had been changed.

The E1 and E0 bits control the error checking which should be carried out on packets 1 to 23 when the page being requested is captured.

For a multi-page device, each packet can only be written into one place in the teletext RAM, so if a page matches more than one of the page requests the data is written into the area of memory corresponding to the lowest numbered matching page request.

At power-up each page request defaults to any page, hold on and error check Mode 0.

Start Column	Byte Identification	PRD<4>	PRD<3>	PRD<2>	PRD<1>	PRD<0>
0	Magazine	DO CARE	HOLD	MAG2	MAG1	MAG0
1	Page Tens	DO CARE	PT3	PT2	PT1	PT0
2	Page Units	DO CARE	PU3	PU2	PU1	PU0
3	Hours Tens	DO CARE	x	x	HT1	HT0
4	Hours Units	DO CARE	HU3	HU2	HU1	HU0
5	Minutes Tens	DO CARE	x	MT2	MT1	MT0
6	Minutes Units	DO CARE	MU3	MU2	MU1	MU0
7	Error Mode	x	x	x	E1	E0

Table 13 The contents of the Page Request RAM

Note: MAG = Magazine PT = Page Tens PU = Page Units HT = Hours Tens HU = Hours Units

MT = Minutes Tens MU = Minutes Units E = Error check mode

Rolling Headers and Time

When a new page has been requested it is conventional for the decoder to turn the header row of the display green and to display each page header as it arrives until the correct page has been found.

When a page request is changed (i.e. when the TXT3 SFR is written to) a flag (PBLF) is written into bit 5, column 9, row 25 of the corresponding block of the page memory. The state of the flag for each block is updated every TV line, if it is set for the current display block, the acquisition section writes all valid page headers which arrive

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into the display block and automatically writes an alphanumeric green character into column 7 of row 0 of the display block every TV line.

When a requested page header is acquired for the first time, rows 1 to 23 of the relevant memory block are cleared to space, i.e. have 20H written into every column, before the rest of the page arrives. Row 24 is also cleared if the TXT0.X24 POSN bit is set. If the TXT1.EXT PKT OFF bit is set the extension packets corresponding to the page are also cleared.

The last 8 characters of the page header are used to provide a time display and are always extracted from every valid page header as it arrives and written into the display block.

The TXT0.DISABLE HEADER ROLL bit prevents any data being written into row 0 of the page memory except when a page is acquired off air i.e. rolling headers and time are not written into memory. The TXT1.ACQ OFF bit prevents any data being written into the memory by the teletext acquisition section.

When a parallel magazine mode transmission is being received only headers in the magazine of the page requested are considered valid for the purposes of rolling headers and time. Only one magazine is used even if a don't care magazine is requested. When a serial magazine mode transmission is being received all page headers are considered to be valid.

ERROR CHECKING

Before teletext packets are written in to the page memory they are error checked. The error checking carried out depends on the packet number, the byte number, the error check mode bits in the page request data and the TXT1.8-BIT bit.

If an uncorrectable error occurs in one of the Hamming checked addressing and control bytes in the page header or in the Hamming checked bytes in packet 8/30, bit 4 of the byte written into the memory is set, to act as an error flag to the software. If uncorrectable errors are detected in any other Hamming checked data the byte is not written into the memory.

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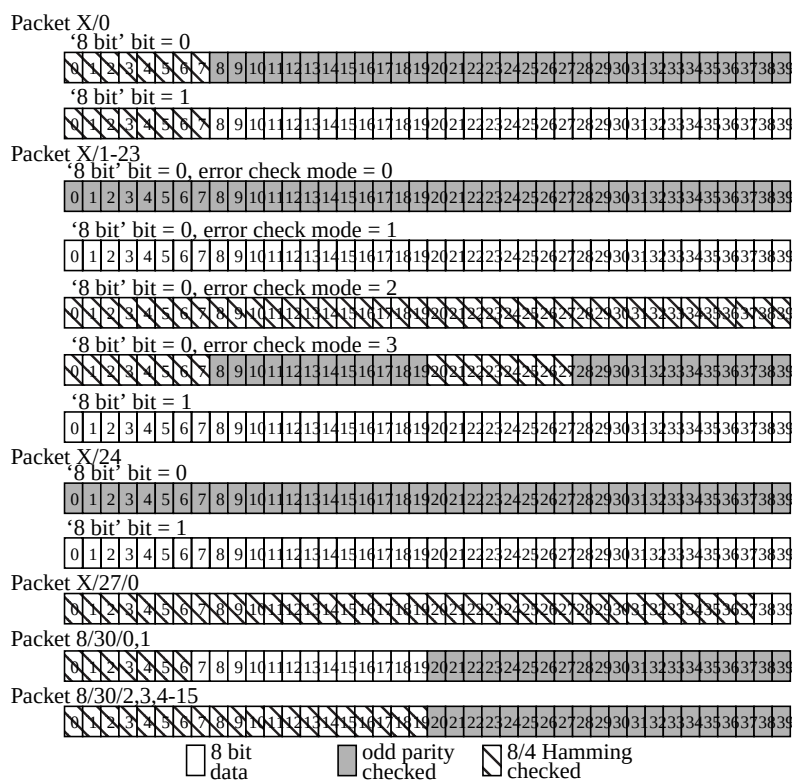


Figure 19 Error Checking

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Basic Page Blocks (0 to 8/9)

	0	6	7	8	39
Row 0	OSD only	6w	8g		Packet X/0
1					Packet X/1
2					Packet X/2
3					Packet X/3
4					Packet X/4
5					Packet X/5
6					Packet X/6
7					Packet X/7
8					Packet X/8
9					Packet X/9
10					Packet X/10
11					Packet X/11
12					Packet X/12
13					Packet X/13
14					Packet X/14
15					Packet X/15
16					Packet X/16
17					Packet X/17
18					Packet X/18
19					Packet X/19
20					Packet X/20
21					Packet X/21
22					Packet X/22
23					Packet X/23
24					Packet X/24 ¹
25	Control Data	9	VPS Data ²	23	

NOTE: ¹ if 'X24 Posn' bit = 1.
² VPS data block 9, unused in blocks 0 - 8.

Figure 20 Teletext Packet Storage Locations

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Teletext Memory Organisation

The teletext memory is divided into 10 blocks. Normally, when the TXT1.EXT PKT OFF bit is logic 0, each of blocks 0 to 8 contain a teletext page arranged in the same way as the basic page memory of the page device and block 9 contains extension packets. When the TXT1.EXT PKT OFF bit is logic 1, no extension packets are captured and block 9 of the memory is used to store another page. The number of the memory block into which a page is written corresponds to the page request number which resulted in the capture of the page.

Packet 0, the page header, is split into 2 parts when it is written into the text memory. The first 8 bytes of the header contain control and addressing information. They are Hamming decoded and written into columns 0 to 7 of row 25. Row 25 also contains the magazine number of the acquired page and the PBLF flag but the last 13 bytes are unused and may be used by the software. Row 25, column 10 is reserved and should not be used by software.

Extension Packet Block (9)

Row 0	Packet X/24 for page in block 0 *
1	Packet X/27/0 for page in block 0
2	Packet 8/30/0,1
3	Packet 8/30/2,3
4	Packet X/24 for page in block 1 *
5	Packet X/27/0 for page in block 1
6	Packet X/24 for page in block 2 *
7	Packet X/27/0 for page in block 2
8	Packet X/24 for page in block 3 *
9	Packet X/27/0 for page in block 3
10	Packet X/24 for page in block 4 *
11	Packet X/27/0 for page in block 4
12	Packet X/24 for page in block 5 *
13	Packet X/27/0 for page in block 5
14	Packet X/24 for page in block 6 *
15	Packet X/27/0 for page in block 6
16	Packet X/24 for page in block 7 *
17	Packet X/27/0 for page in block 7
18	Packet X/24 for page in block 8 *
19	Packet X/27/0 for page in block 8
20	Packet 8/30/4-15
21	
22	
23	
24	
25	VPS Data

NOTE* if 'X24 Posn' bit = 0

Figure 21 Teletext Extension Packet Storage Locations

ROW 25 DATA CONTENTS

The Hamming error flags are set if the on-board 8/4 Hamming checker detects that there has been an uncorrectable (2 bit) error in the associated byte. It is possible for the page to still be acquired if some of the page address information contains uncorrectable errors if that part of the page request was a 'don't care'. There is no error flag for the magazine number as an uncorrectable error in this information prevents the page being acquired.

The interrupted sequence (C9) bit is automatically dealt with by the acquisition section so that rolling headers do not contain a discontinuity in the page number sequence.

The magazine serial (C11) bit indicates whether the transmission is a serial or a parallel magazine transmission. This affects the way the acquisition section operates and is dealt with automatically.

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The newflash (C5), subtitle (C6), suppress header (C7), inhibit display (C10) and language control (C12 to 14) bits are dealt with automatically by the display section, described below.

The update (C8) bit has no effect on the hardware. The remaining 32 bytes of the page header are parity checked and written into columns 8 to 39 of row 0. Bytes which pass the parity check have the MSB set to logic 0 and are written into the page memory. Bytes with parity errors are not written into the memory.

Col	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	0	Hamming error	PU3	PU2	PU1	PU0
1	0	0	0	Hamming error	PT3	PT2	PT1	PT0
2	0	0	0	Hamming error	MU3	MU2	MU1	MU0
3	0	0	0	Hamming error	C4	MT2	MT1	MT0
4	0	0	0	Hamming error	HU3	HU2	HU1	HU0
5	0	0	0	Hamming error	C6	C5	HT1	HT0
6	0	0	0	Hamming error	C10	C9	C8	C7
7	0	0	0	Hamming error	C14	C13	C12	C11
8	0	0	0	FOUND	0	Mag2	Mag1	Mag0
9	0	0	PBLF	0	0	0	0	0
10 : 23				UNUSED				

Table 14 The data in row 25 of the basic memory

Mag = Magazine
PT = Page Tens
PU = Page Units
HT = Hours Tens
HU = Hours Units
MT = Minutes Tens

C4 = Erase page
C5 = Newsflash
C6 = Subtitle
C7 = Suppress Header
C8 = Update
MU = Minutes Units

C9 = Interrupted Sequence
C10 = Inhibit Display
C11 = Magazine Serial
C12-14 = Language Selection

INVENTORY PAGE

If the TXT0.INV on bit is 1, memory block 8 is used as an inventory page. The inventory page consists of two tables, - the Transmitted Page Table (TPT) and the subtitle page table (SPT).

In each table, every possible combination of the page tens and units digit, 00 to FFh, is represented by a byte. Each bit of these bytes corresponds to a magazine number so each page number, from 100 to 8FF, is represented by a bit in the table. The bit for a particular page in the TPT is set when a page header is received for that page. The bit in the SPT is set when a page header for the page is received which has the 'subtitle' page header control bit (C6) set. The bit for a particular page in the TPT is set when a page header is received for that page. The bit in the SPT is set when a page header for the page is received which has the 'subtitle' page header control bit (C6) set.

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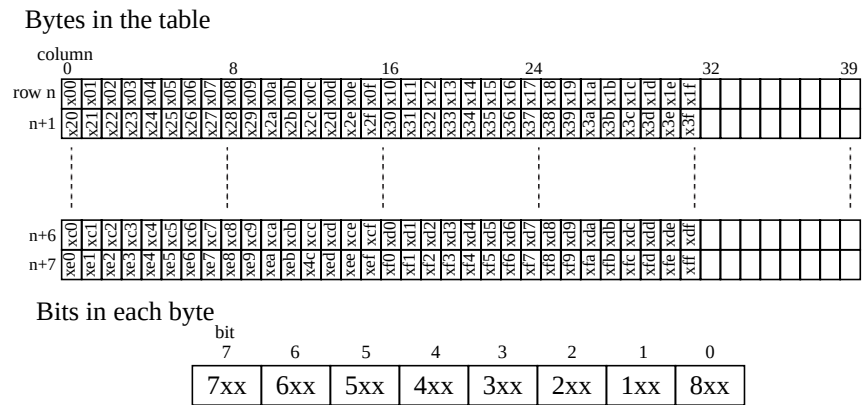


Figure 22 SPT/TPT Organisation

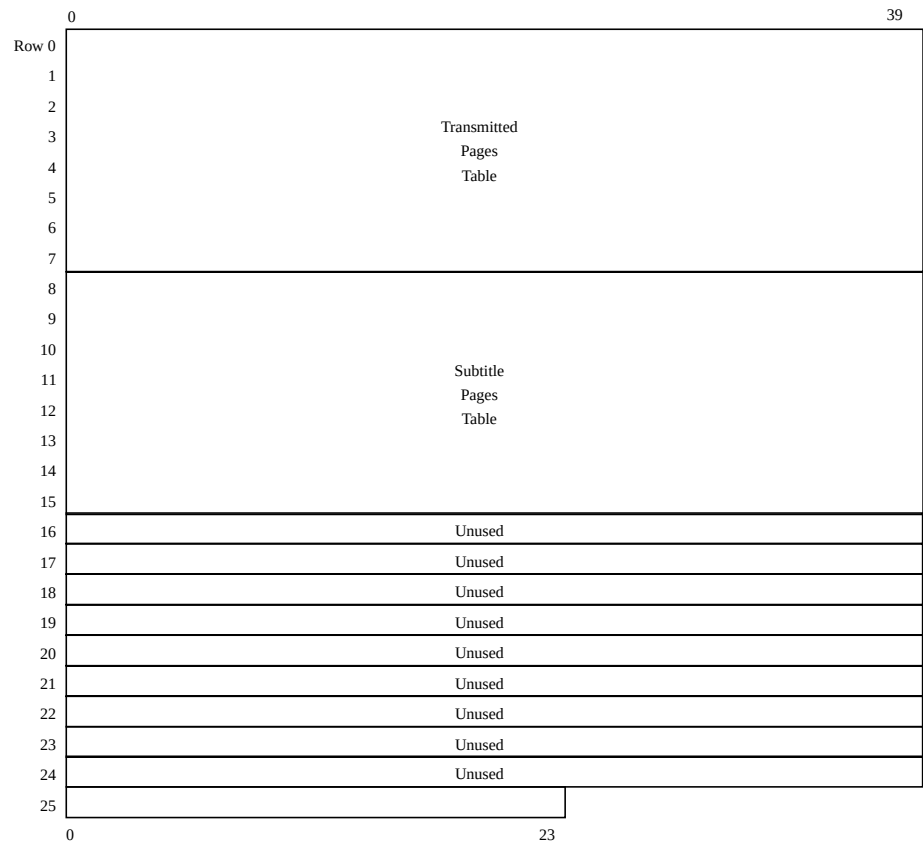


Figure 23 Inventory page Organisation

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PACKET 26 PROCESSING

One of the uses of packet 26 is to transmit characters which are not in the basic teletext character set. The family automatically decodes packet 26 data and, if a character corresponding to that being transmitted is available in the character set, automatically writes the appropriate character code into the correct location in the teletext memory. This is not a full implementation of the packet 26 specification allowed for in level 2 teletext, and so is often referred to as level 1.5.

By convention, the packets 26 for a page are transmitted before the normal packets. To prevent the default character data over writing the packet 26 data the device incorporates a mechanism which prevents packet 26 data from being overwritten. This mechanism is disabled when the Spanish national option is detected as the Spanish transmission system sends even parity (i.e. incorrect) characters in the basic page locations corresponding to the characters sent via packet 26 and these will not over write the packet 26 characters anyway. The special treatment of Spanish national option is prevented if TXT12. ROM VER R4 is logic 0 or if the TXT8.DISABLE SPANISH is set.

Packet 26 data is processed regardless of the TXT1. EXT PKT OFF bit, but setting the TXT1.X26 OFF disables packet 26 processing.

The TXT8. Packet 26 received bit is set by the hardware whenever a character is written into the page memory by the packet 26 decoding hardware. The flag can be reset by writing a logic 0 into the SFR bit.

525 LINE WORLD SYSTEM TELETEXT

The 525 line format is similar to the 625 line format but the data rate is lower and there are less data bytes per packet (32 rather than 40). There are still 40 characters per display row so extra packets are sent each of which contains the last 8 characters for four rows. These packets can be identified by looking at the 'tabulation bit' (T), which replaces one of the magazine bits in 525 line teletext. When an ordinary packet with T = 1 is received, the decoder puts the data into the four rows starting with that corresponding to the packet number, but with the 2 LSBs set to 0. For example, a packet 9 with T = 1 (packet X/1/9) contains data for rows 8, 9, 10 and 11. The error checking carried out on data from packets with T = 1 depends on the setting of the TXT1. 8 BIT bit and the error checking control bits in the page request data and is the same as that applied to the data written into the same memory location in the 625 line format.

The rolling time display (the last 8 characters in row 0) is taken from any packets X/1/1, 2 or 3 received. In parallel magazine mode only packets in the correct magazine are used for rolling time. Packet number X/1/0 is ignored.

The tabulation bit is also used with extension packets. The first 8 data bytes of packet X/1/24 are used to extend the Fastext prompt row to 40 characters. These characters are written into whichever part of the memory the packet 24 is being written into (determined by the 'X24 Posn' bit).

Packets X/0/27/0 contain 5 Fastext page links and the link control byte and are captured, Hamming checked and stored by in the same way as are packets X/27/0 in 625 line text. Packets X/1/27/0 are not captured.

Because there are only 2 magazine bits in 525 line text, packets with the magazine bits all set to 0 are referred to as being in magazine 4. Therefore, the broadcast service data packet is packet 4/30, rather than packet 8/30. As in 625 line text, the first 20 bytes of packet 4/30 contain encoded data which is decoded in the same way as that in packet 8/30. The last 12 bytes of the packet contains half of the parity encoded status message. Packet 4/0/30 contains the first half of the message and packet 4/1/30 contains the second half. The last 4 bytes of the message are not written into memory. The first 20 bytes of the each version of the packet are the same so they are stored whenever either version of the packet is acquired.

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In 525 line text each packet 26 only contains ten 24/18 Hamming encoded data triplets, rather than the 13 found in 625 line text. The tabulation bit is used as an extra bit (the MSB) of the designation code, allowing 32 packet 26s to be transmitted for each page. The last byte of each packet 26 is ignored.

	0	6	7	8	g	39
Row 0	OSD only			αw/0	Packet X/0/0	Rolling Time
1					Packet X/0/1	Packet X/1/1
2					Packet X/0/2	
3					Packet X/0/3	
4					Packet X/0/4	Packet X/1/4
5					Packet X/0/5	
6					Packet X/0/6	
7					Packet X/0/7	
8					Packet X/0/8	Packet X/1/8
9					Packet X/0/9	
10					Packet X/0/10	
11					Packet X/0/11	
12					Packet X/0/12	Packet X/1/12
13					Packet X/0/13	
14					Packet X/0/14	
15					Packet X/0/15	
16					Packet X/0/16	Packet X/1/16
17					Packet X/0/17	
18					Packet X/0/18	
19					Packet X/0/19	
20					Packet X/0/20	Packet X/1/20
21					Packet X/0/21	
22					Packet X/0/22	
23					Packet X/0/23	
24					Packet X/0/24 †	Packet X/1/24 †
25	Control Data					
	0	9		23		† if 'X24 Posn' bit = 1

Figure 24 Teletext Packet Storage for 525WST

**TV signal processor-Teletext decoder with
embedded μ -Controller**

TDA 935X/6X/8X series**Display**

The display section is based on the requirements for a Level 1.5 WST Teletext and US Closed Caption. There are some enhancements for use with locally generated On-Screen Displays.

The display section reads the contents of the Display memory and interprets the control/character codes. From this information and other global settings, the display produces the required RGB signals and Video/Data (Fast Blanking) signal.

Display Features

- Teletext and Enhanced OSD modes
- Level 1.5 WST features
- US Closed Caption Features
- Serial and Parallel Display Attributes
- Single/Double/Quadruple Width and Height for characters
- Scrolling of display region
- Variable flash rate controlled by software
- Globally selectable scan lines per row 9/10/13/16
- Globally selectable character matrix (HxV) 12x9, 12x10, 12x13, 12x16
- Italics
- Soft Colours using CLUT with 4096 colour palette
- Underline
- Overline
- Fringing (Shadow) selectable from N-S-E-W direction
- Fringe colour selectable
- Meshing of defined area
- Contrast reduction of defined area
- Cursor
- Special Graphics characters with two planes, allowing four colours per character
- 32 Software re-definable On-Screen Display characters
- 4 WST Character sets(G0/G2) in single device (e.g. Latin,Cyrillic,Greek,Arabic)
- G1 Mosaic graphics, Limited G3 Line drawing characters
- WST Character sets and Closed Caption Character set in single device

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Display Block Diagram

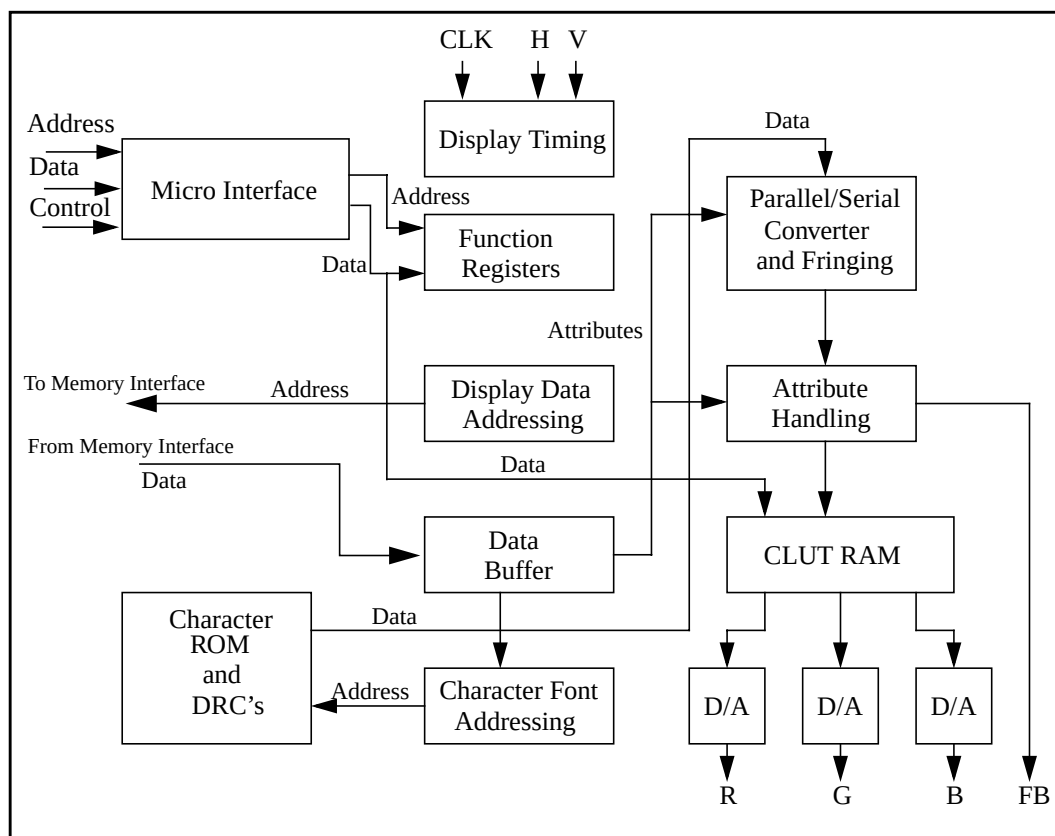


Figure 25 Display Block Diagram

Display Modes

The display section has two distinct modes with different features available in each. The two modes are:

- **TXT:-** This is the display configured as the WST mode with additional serial and global attributes to enable the same functionality as the SAA5497 (ETT) device. The display is configured as a fixed 25 rows with 40 characters per row.
- **CC:-** This is the display configured as the US Closed Caption mode with the same functionality as the PC83C771 device. The display is configured as a maximum of 16 rows with a maximum of 48 characters per row.

In both of the above modes the Character matrix, and TV lines per row can be defined. There is an option of 9/10/13/16 TV lines per display row, and a Character matrix (HxV) of 12x9, 12x10, 12x13, or 12x16. Not all combinations of TV lines per row and maximum display rows give a sensible OSD display, since there is limited number of TV scan lines available.

Special Function Register, TXT21 and memory mapped registers are used to control the mode selection. Throughout this section, the features will be described, and their function in each mode given. If the feature is different in either mode then this is stated.

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Features available in each mode

The following is a list of features available in each mode, and whether it is a serial or parallel attribute, or if it has a global effect on the display.

Feature	TXT	CC
Flash	serial	serial
Boxes	Txt/OSD (Serial)	serial
Horizontal Size	x1/x2/x4 (serial)	x1/x2 (serial)
Vertical Size	x1/x2 (serial) x4 (global)	x1/x2 (serial)
Italic	N/A	serial
Foreground colours	8 (serial)	8+8 (parallel)
Background colours	8 (serial)	16 (serial)
Soft Colours (CLUT)	16 from 4096	16 from 4096
Underline	N/A	serial
Overline	N/A	serial
Fringe	N+S+E+W	N+S+E+W
Fringe Colour	16 (Global)	16 (Serial)
Meshing of Background	Black or Colour (Global)	All (Global)
Fast Blanking Polarity	YES	YES
Screen Colour	16 (Global)	16 (Global)
DRCS	32 (Global)	32/16 (Global)
Character Matrix (HxV)	12x9/10/13/16	12x9/10/13/16
No. of Rows	25	16
No. of Columns	40	48
No of Characters displayable	1000	544
Cursor	YES	YES
Special Graphics (2 planes per character)	16	16
Scroll	NO	YES

Table 15 Display Features

Display Feature Descriptions

All display features are now described in detail for both TXT and CC modes.

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

FLASH

Flashing causes the foreground colour pixel to be displayed as the background pixels. The flash frequency is controlled by software setting and resetting display register REG0: Status (see) at the appropriate interval.

CC:- This attribute is valid from the time set (see Table 21) until the end of the row or until otherwise modified.

TXT:- This attribute is set by the control character 'flash' (08h) (see Figure 31) and remains valid until the end of the row or until reset by the control character 'steady' (09h).

BOXES

CC:- This attribute is valid from the time set until end of row or otherwise modified if set with Serial Mode 0. If set with Serial Mode 1, then it is set from the next character onwards.

In text mode (within CC mode) the background colour is displayed regardless of the setting of the box attribute bit. Boxes take affect only during mixed mode, where boxes are set in this mode the background colour is displayed. Character locations where boxes are not set show video/screen colour (depending on the setting in the display control register. REG0: Display Control) in stead of the background colour.

TXT:- Two types of boxes exist the Teletext box and the OSD box. The Teletext box is activated by the 'start box' control character (0Bh), Two start box characters are required begin a Teletext box, with box starting between the 2 characters. The box ends at the end of the line or after a 'end box' control character.

TXT mode can also use OSD boxes, they are started using size implying OSD control chracters(BCh/BDh/BEh/BFh). The box starts after the control character ('set after') and ends either at the end of the row or at the next size implying OSD character ('set at'). To allow OSD boxes to be placed over teletext page the attributes flash, teletext box, conceal, separate graphics, twist and hold graphics are all reset at the start of an OSD box, as they are at the start of the row. OSD Boxes are only valid in TV mode which is defined by TXT5=03h and TXT6=03h.

SIZE

The size of the characters can be modified in both the horizontal and vertical directions.

CC:- Two sizes are available in both the horizontal and vertical directions. The sizes available are normal (x1), double(x2) height/width and any combination of these. The attribute setting is always valid for the whole row. Mixing of sizes is within a row is not possible.

TXT:- Three horizontal sizes are available normal (x1),double (x2),quadruple (x4). The control characters 'normal size' (0Ch/BCh) enables normal size, the 'double width' or double size (0Eh/BEh/0Fh/BFh) enables double width characters. Any two consecutive combination of 'double width' or 'double size' (0Eh/BEh/0Fh/Bfh) activates quadruple width characters, provided quadruple width characters are enabled by TXT4.Quad Width Enable.

Three vertical sizes are available normal(x1),double(x2),quadruple(x4). The control characters 'normal size' (0Ch/BCh) enable normal size, the 'double height' or 'double size' (0Dh/BDh/0Fh/BFh) enable double height characters. Quadruple height character are achieved by using double height characters and setting the global attributes TXT7.Double Height(expand) and TXT7.Bottom/Top.

ITALIC

CC:- This attribute is valid from the time set until the end of the row or otherwise modified. The attribute causes the character foreground pixels to be offset horizontally by 1 pixel per 4 scan lines (interlaced mode). The base is the bottom left character matrix pixel. The pattern of the character is indented as shown in Figure 26.

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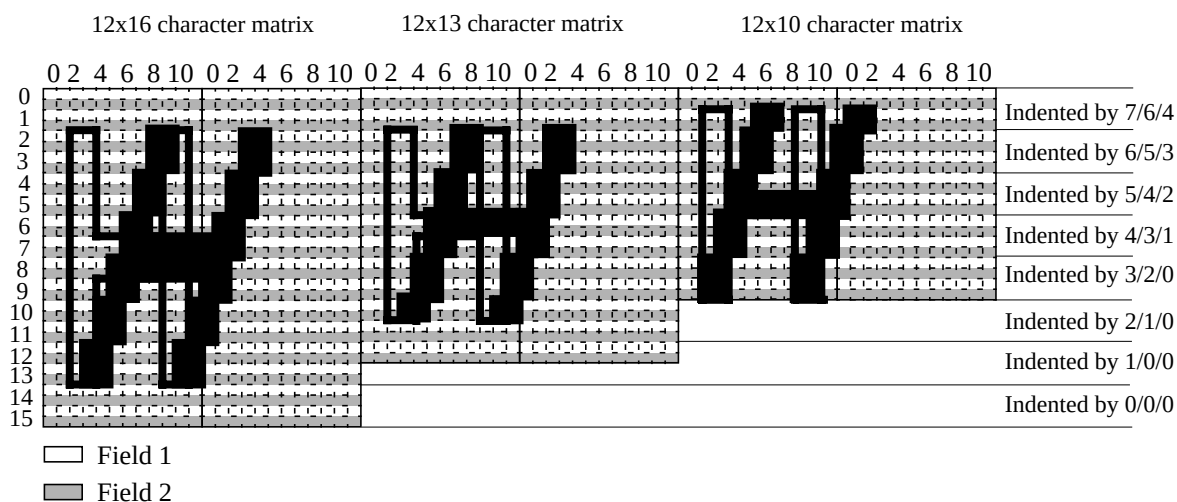


Figure 26 Italic Characters

TXT:- The Italic attribute is not available.

COLOURS

CLUT (Colour Look Up Table)

A CLUT (Colour Look Up Table) with 16 colour entries is provided. The colours are programmable out of a palette of 4096 (4 bits per R, G and B). The CLUT is defined by writing data to a RAM that resides in the MOVX address space of the 80C51

RED3-0 b11... b8	GRN3-0 b7... b4	BLU3-0 b3... b0	Colour entry
0 0 0 0	0 0 0 0	0 0 0 0	0
0 0 0 0	0 0 0 0	1 1 1 1	1
...	...	...	...
1 1 1 1	1 1 1 1	0 0 0 0	14
1 1 1 1	1 1 1 1	1 1 1 1	15

Table 16 CLUT Colour values

Foreground Colour

CC:- The foreground colour can be chosen from 8 colours on a character by character basis. Two sets of 8 colours are provided. A serial attribute switches between the banks (see Table 21 Serial Mode 1, bit 7). The colours are the CLUT entries 0 to 7 or 8 to 15.

TXT:- The foreground colour is selected via a control character (see Figure 31). The colour control characters

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takes effect at the start of the next character ('Set After') and remain valid until the end of the row, or until modified by a control character. Only 8 foreground colours are available.

The TEXT foreground control characters map to the CLUT entries as shown in Table 17.

Control Code	Defined Colour	CLUT Entry
00h	Black	0
01h	Red	1
02h	Green	2
03h	Yellow	3
04h	Blue	4
05h	Magenta	5
06h	Cyan	6
07h	White	7

Table 17 Foreground CLUT mapping

Background Colour

CC:- This attribute is valid from the time set until end of row or otherwise modified if set with Serial Mode 0. If set with Serial Mode 1, then the colour is set from the next character onwards. The background colour can be chosen from all 16 CLUT entries.

TXT:- The control character 'New background' (1Dh) is used to change the background colour to the current foreground colour. The selection is immediate ('Set at') and remains valid until the end of the row or until otherwise modified.

The TEXT background control characters map to the CLUT entries as shown in Table 18.

Control Code	Defined Colour	CLUT Entry
00h+1Dh	Black	8
01h+1Dh	Red	9
02h+1Dh	Green	10
03h+1Dh	Yellow	11
04h+1Dh	Blue	12
05h+1Dh	Magenta	13
06h+1Dh	Cyan	14
07h+1Dh	White	15

Table 18 Background CLUT mapping

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BACKGROUND DURATION

The attribute when set takes effect from the current position until to the end of the text display defined in the MMR REG4:Text Area End.

CC:- The background duration attribute (see Table 21 Serial Mode 1, bit 8) in combination with the End Of Row attribute (see Table 21 Serial Mode 1, bit 9) forces the background colour to be display on the row until the end of the text area is reached

TXT:- This attribute is not available.

UNDERLINE

The underline attribute causes the characters to have the bottom scan line of the character cell forced to foreground colour, including spaces. If background duration is set, then underline is set until the end of the text area

CC/OSD:- The underline attribute (see Table 21 Serial Mode 0/1, bit 4) is valid from the time set until end of row or otherwise modified.

TXT:- This attribute is not available, Row length is fixed to 40 characters.

OVERLINE

The overline attribute causes the characters to have the top scan line of the character cell forced to foreground colour, including spaces. If background duration is set, then overline is set until the end of the text area

CC/OSD:- The overline attribute (see Table 21 Serial Mode 0/1, bit 5) is valid from the time set until end of row or otherwise modified. Over-lining of Italic characters is not possible

TXT:- This attribute is not available.

END OF ROW

CC/OSD:- The number of characters in a row is flexible and can determined by the end of row attribute (see Table 21 Serial Mode 1, bit 9). There must exist a space character 20H between the End of Row attribute and the start of the subsequent display row. The maximum number of characters positioned displayed is determined by the setting of the MMR REG2:Text Position Horizontal and the MMR REG4:Text Area End.

TXT:- This attribute is not available, Row length is fixed at 40 characters.

FRINGING

A fringe (shadow) can be defined around characters. The fringe direction is individually selectable in any of the North, South, East and West direction using REG3:Fringing Control. The colour of the fringe can also be defined as one of the entries in the CLUT, again using REG3:Fringing Control.

CC/OSD:- The fringe attribute (see Table 21 Serial Mode 0, bit 9) is valid from the time set until the end of the row or otherwise modified.

TXT:- The display of fringing in TXT mode is controlled by the TXT4.SHADOW bit. When set all the alphanumeric characters being displayed are shadowed, graphics characters are not shadowed.

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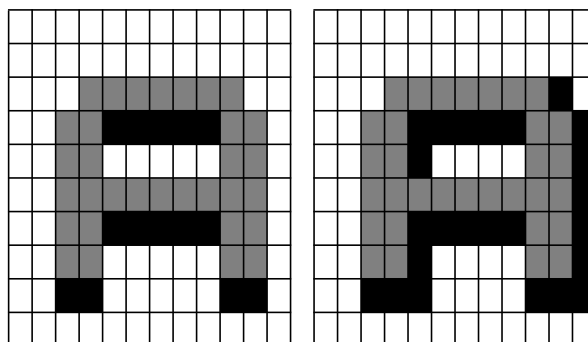


Figure 27 South and Southwest Fringing

MESHING

The attribute effects the background colour being displayed. Alternate pixels are displayed as the background colour or video. The structure is offset by 1 pixel from scan line to scan line, thus achieving a checker board display of the background colour and video.

TXT:- There are two meshing attributes one that only affects black background colours TXT4.BMESH and a second that only affects backgrounds other than black TXT4.CMESH. A black background is defined as CLUT entry 8, a none black background is defined as CLUT entry 9 to 15.

CC:- The setting of the Mesh bit in REG0:Display Control has the effect of meshing any background colour.

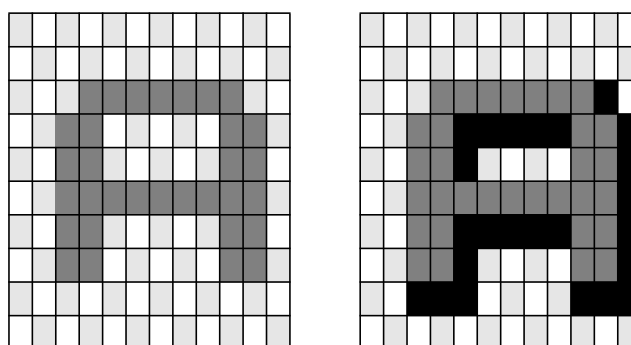


Figure 28 Meshing and Meshing/Fringing(South+West)

Note: There is a restriction on the use of fringing (shadowing) when combined with meshing. This applies to both black and coloured meshing. The limitation is that when meshing is enabled, only the text pixels will be fringed and video pixels are displayed without fringing.

CURSOR

The cursor operates by reversing the background and foreground colours in the character position pointed to by the active cursor position. The cursor is enabled using TXT7.CURSOR ON. When active, the row the cursor appears on is defined by TXT9.R<4:0> and the column is defined by TXT10.C<5:0>. The position of the cursor can be fixed using TXT9.CURSOR FREEZE

CC:- The valid range for row is 0 to 15. The valid range for column is 0 to 47. The cursor remains rectangular

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at all times, its shape is not affected by the italic attribute, therefore it is not advised to use the cursor with italic characters.

TXT:- The valid range for row is 0 to 24. The valid range for column is 0 to 39.



Figure 29 Cursor display

SPECIAL GRAPHICS CHARACTERS

CC/TXT:- Several special characters are provided for improved OSD effects. These characters provide a choice of 4 colours within a character cell. The total number of special graphics characters is limited to 16. They are stored in the character codes 8Xh and 9Xh of the character table (32 ROM characters), or in the DRC's which overlay character codes 8Xh and 9Xh. Each special graphics character uses two consecutive normal characters.

Fringing, underline and overline is not possible for special graphics characters. Special graphics characters are activated when `TXT1.OSD_PLANES = 1`.

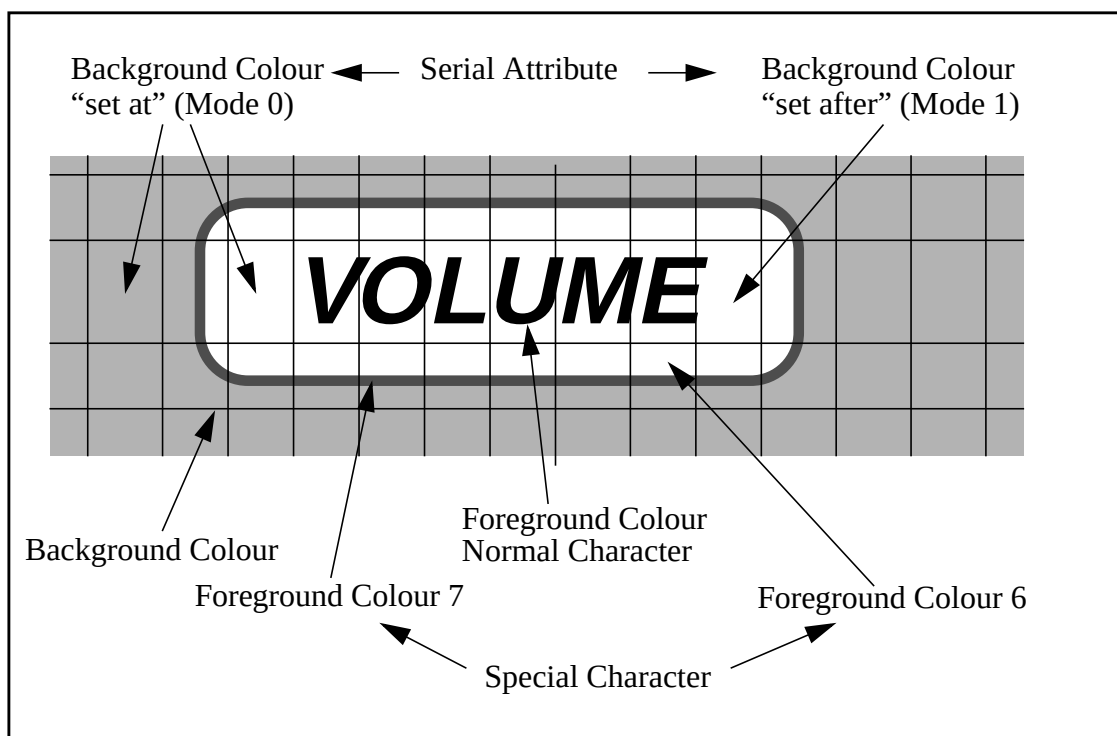


Figure 30 Special Character Example

The example in Figure 30 could be done with 8 special characters.

TV signal processor-Teletext decoder with embedded μ -Controller

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If the screen colour is transparent (implicit in mixed mode) and inside the object the box attribute is set, then the object is surrounded by video. If the box attribute is not set the background colour inside the object will also be displayed as transparent.

Plane 1	Plane 0	Colour Allocation
0	0	Background Colour
0	1	Foreground Colour
1	0	CLUT entry 6
1	1	CLUT entry 7

Table 19 Special character colour allocation

Character and Attribute Coding

This section describes the character and attribute coding for each mode.

CC MODE

Character coding is split into character oriented attributes (parallel) and character group coding (serial). The serial attributes take effect either at the position of the attribute (set at), or at the following location (set after) and remain effective until either modified by a new serial attribute or until the end of the row. A serial attribute is represented as a space (the space character itself however is not used for this purpose), the attributes that are still active, e.g. overline and underline will be visible during the display of the space.

The default setting at the start of a row is:

- 1x size
- flash OFF
- overline OFF
- underline OFF
- italics OFF
- Display mode = superimpose
- fringing OFF
- background colour duration = 0
- end of row = 0

The coding is done in 12 bit words. The codes are stored sequentially in the display memory. A maximum of 768 character positions can be defined for a single display.

**TV signal processor-Teletext decoder with
embedded μ -Controller**

TDA 935X/6X/8X series*Parallel Character Coding*

Bits	Description
0-7	8 bit character code
8-10	3 bits for 8 foreground colours
11	Mode bit: 0 = Parallel code

Table 20 Parallel Character Coding

TV signal processor-Teletext decoder with embedded μ -Controller

TDA 935X/6X/8X series

Serial Character Coding

Bits	Description		
	Serial Mode 0 ("set at")	Serial Mode 1	
		Char.Pos. 1 ("set at")	Char.Pos. >1 ("set after")
0-3	4 bits for 16 Background colours	4 bits for 16 Background colours	4 bits for 16 Background colours
4	0 = Underline OFF 1 = Underline ON	Horizontal Size: 0 = normal 1 = x2	0 = Underline OFF 1 = Underline ON
5	0 = Overline OFF 1 = Overline ON	Vertical Size: 0 = normal 1 = x2	0 = Overline OFF 1 = Overline ON
6	Display mode: 0 = Superimpose 1 = Boxing	Display mode: 0 = Superimpose 1 = Boxing	Display mode: 0 = Superimpose 1 = Boxing
7	0 = Flash OFF 1 = Flash ON	Foreground colour switch 0 = Bank 0 (colours 0-7) 1 = Bank 1 (colours 8-15)	Foreground colour switch 0 = Bank 0 (colours 0-7) 1 = Bank 1 (colours 8-15)
8	0 = Italics OFF 1 = Italics ON	Background colour duration: 0 = stop BGC 1 = set BGC to end of row	Background colour duration (set at): 0 = stop BGC 1 = set BGC to end of row
9	0 = Fringing OFF 1 = Fringing ON	End of Row 0 = Continue Row 1 = End Row	End of Row (set at): 0 = Continue Row 1 = End Row
10	Switch for Serial coding mode 0 and 1: 0 = mode 0	Switch for Serial coding mode 0 and 1: 1 = mode 1	Switch for Serial coding mode 0 and 1: 1 = mode 1
11	Mode bit: 1 = Serial code	Mode bit: 1 = Serial code	Mode bit: 1 = Serial code

Table 21 Serial Character Coding

TXT MODE

Character coding is in a serial format, with only one attributes being changed at any single location. The serial attributes take effect either at the position of the attribute (Set At), or at the following location (Set After). The attribute remains effective until either modified by new serial attributes or until the end of the row.

TV signal processor-Teletext decoder with embedded μ -Controller

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The default settings at the start of a row is:

- foreground colour white (CLUT Address 7)
- background colour black (CLUT Address 8)
- Horizontal size x1, Vertical size x1 (normal size)
- Alphanumeric ON
- Contiguous Mosaic Graphics
- Release Mosaics
- Flash OFF
- Box OFF
- Conceal OFF
- Twist OFF

The attributes have individual codes which are defined in the basic character table shown in Figure 31.

		bits																$E/\overline{W} = 0$			$E/\overline{W} = 1$			
		b7 b6 b5 b4 b3 b2 b1 b0																1 1 1			1 1 1			
		column																D E F			D E F			
row	code	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	A	B	C						
	bits	alpha black	graphics black			0		Nat Opt	P		Nat Opt	p		O_D	O_D	#	bkgnd black	ú						
	0000	1	alpha red	graphics red	!	1	A	Q	a		q			O_D	O_D	\$	bkgnd red	Á						
	0010	2	alpha green	graphics green	"	2	B	R	b		r			O_D	O_D	x	bkgnd green	É						
	0011	3	alpha yellow	graphics yellow		3	C	S	c		s			O_D	O_D	2	bkgnd yellow	í						
	0100	4	alpha blue	graphics blue		4	D	T	d		t			O_D	O_D	ä	bkgnd blue	ó						
	0101	5	alpha magenta	graphics magenta	%	5	E	U	e		u			O_D	O_D	ë	bkgnd magenta	ú						
	0110	6	alpha cyan	graphics cyan	&	6	F	V	f		v			O_D	O_D	ö	bkgnd cyan	ð						
	0111	7	alpha white	graphics white	'	7	G	W	w					O_D	O_D	ü	bkgnd white	ş						
	1000	8	flash	conceal display	(	8	H	X	h		x			O_D	O_D	Ä	ö	ş						
	1001	9	steady	contiguous graphics	)	9	I	Y	i		y			O_D	O_D	È	ü	ä						
	1010	A	end box	separated graphics	*		J	Z	j		z			O_D	O_D	Ö	ö	ï						
	1011	B	start box		+		K			Nat Opt	k		Nat Opt	O_D	O_D	Ü	Ü	ö						
	1100	C	normal height	black bkgnd	,		L		Nat Opt	l		Nat Opt		O_D	O_D	á	norm sz OSD	Ä						
	1101	D	double height	new bkgnd	-		M		Nat Opt	m		Nat Opt		O_D	O_D	é	dbl ht OSD	È						
	1110	E	double width	hold graphics	.		N		Nat Opt	n		Nat Opt		O_D	O_D	í	dbl wd OSD	ä						
	1111	F	double size	release graphics	/		O		Nat Opt	o				O_D	O_D	ó	dbl sz OSD	Ä						

Figure 31 TXT Basic Character Set

Screen and Global Controls

A number of attributes are available that affect the whole display region, and cannot be applied selectively to regions of the display.

TV signal processor-Teletext decoder with embedded μ -Controller

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TV SCAN LINES PER ROW

The number of TV scan lines per field used for each display row can be defined, the value is independent of the character size being used. The number of lines can be either 10/13/16 per display row. The number of TV scan lines per row is defined TXT21.DISP_LINES<1:0>.

A value of 9 lines per row can be achieved if the display is forced into 525 line display mode by TXT17.DISP_FORCE<1:0>, or if the device is in 10 line mode and the automatic detection circuitry within display finds 525 line display syncs.

CHARACTER MATRIX (HxV)

There are three different character matrices available, these are 12 x 10, 12 x 13 and 12 x 16. The selection is made using TXT21.CHAR_SIZE<1:0> and is independent of the number of display lines per row.

If the character matrix is less than the number of TV scan lines per row then the matrix is padded with blank lines. If the character matrix is greater than the number of TV scan lines then the character is truncated.

DISPLAY MODES

CC:- When attributes superimpose or boxing (see Table 21 Serial Mode 0/1, bit 6) are set, the resulting display depends on the setting of the following screen control mode bits in the MMR REG0:Display Control.

Display Mode	MOD [1.0]	Description
Video	00	Video mode disables all display activities and sets the RGB to true black and VDS to video.
Full Text	01	Full Text mode displays screen colour at all locations not covered by character foreground or background colour. The box attribute has no effect.
Mixed Screen Colour	10	Mixed Screen mode displays screen colour at all locations not covered by character foreground, within boxed areas or, background colour.
Mixed Video	11	Mixed Video mode displays video at all locations not covered by character foreground, within boxed areas or, background colour.

Table 22 Display Modes

TXT:- The display mode is controlled by the bits in the TXT5 and TXT6. There are 3 control functions - Text on, Background on and Picture on. Separate sets of bits are used inside and outside Teletext boxes so that different display modes can be invoked. TXT6 is used if the newflash (C5) or subtitle (C6) bits in row 25 of the basic page memory are set otherwise TXT5 is used. This allows the software to set up the type of display required on newflash and subtitle pages (e.g. text inside boxes, TV picture outside) this will be invoked without any further software intervention when such a page is acquired

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Picture On	Text On	Background On	Effect
0	0	x	Text mode, black screen
0	1	0	Text mode, background always black
0	1	1	Text mode
1	0	x	Video mode
1	1	0	Mixed text and TV mode
1	1	1	Text mode, TV picture outside text area

Table 23 TXT Display Control Bits

When Teletext box control characters are present in the display page memory, the appropriate Box control bit must be set, TXT7.Boxes On Row 0, TXT7.Boxes On Row 1 - 23 or TXT7.Boxes On Row 24. This allows the display mode to be different inside the Teletext box compared to outside. These bits are present to allow boxes in certain areas of the screen to be disabled. So that Teletext boxes can be used for the display of OSD messages without the danger of subtitles in boxes, which may also be in the display page memory, being displayed. The use of teletext boxes for OSD messages has been superseded in this device by the OSD box concept, but these bits remain to allow teletext boxes to be used, if required.

SCREEN COLOUR

CC:- The screen colour is defined by REG0:Display Control and points to a location in the CLUT table. The screen colour covers the full video width. It is visible when the Full Text or Mixed Screen Colour mode is set and no foreground or background pixels are being displayed.

TXT:- The register bits TXT17.SCREEN COL<2:0> can be used to define a colour to be displayed in place of TV picture and the black background colour. If the bits are all set to 0, the screen colour is defined as 'transparent' and TV picture and background colour are displayed as normal. Otherwise the bits define CLUT entries 9 to 15.

Screen colour is displayed from 10.5 ms to 62.5 ms after the active edge of the HSync input and on TV lines 23 to 310 inclusive, for a 625 line display, and lines 17 to 260 inclusive for a 525 line display.

Text Display Controls

TEXT DISPLAY CONFIGURATION (CC MODE)

Two types of areas are possible. The one area is static and the other is dynamic. The dynamic area allows scrolling of a region to take place. The areas cannot cross each other. Only one scroll region is possible.

Display Map

The display map allows a flexible allocation of data in the memory to individual rows.

Sixteen words are provided in the display memory for this purpose. The lower 10 bits address the first word in the memory where the row data starts. The most significant bit enables the display when not within the scroll (dynamic) area.

The display map memory is fixed at the first 16 words in the closed caption display memory.

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b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Pointer to Row Data											
Reserved, should be set to 0											
Text Display Enable, valid outside Soft Scroll Area											
0 = Disable											
1 = Enable											

Table 24 Display map Bit Allocation

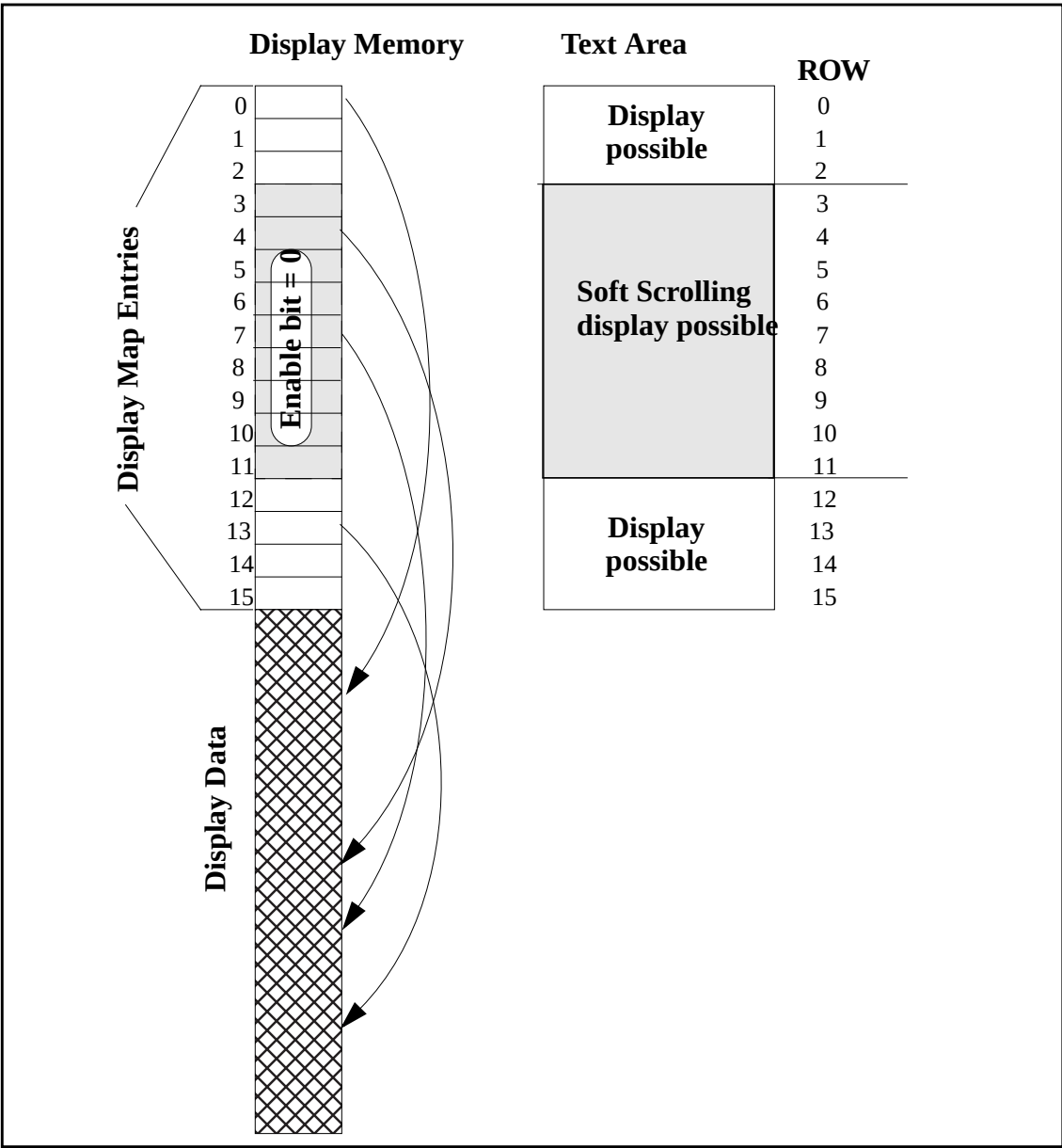


Figure 32 Display Map and Data Pointers

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SOFT SCROLL ACTION

The dynamic scroll region is defined by the following MMRs: REG5:Scroll Area, REG6:Scroll Range, REG14:Top Scroll line and the REG8:Status Register. The scroll area is enabled when the SCON bit is set in MMR REG8: Status.

The position of the soft scroll area window is defined using the Soft Scroll Position (SSP<3:0>), and the height of the window is defined using the Soft Scroll Height (SSH<3:0>), both are in the MMR REG6:Scroll Range. The rows that are scrolled through the window are defined using the Start Scroll Row (STS<3:0>) and the Stop Scroll Row (SPS<3:0>), both are in the MMR REG5:Scroll Area.

The soft scrolling function is done by modifying the Scroll Line (SCL<3:0>) in MMR REG14: Top Scroll Line. and the first scroll row value SCR<3:0> in MMR REG8:Status. If the number of rows allocated to the scroll counter is larger than the defined visible scroll area, this allows parts of rows at the top and bottom to be displayed during the scroll function. The registers can be written throughout the field and the values are updated for display with the next field sync. Care should be taken that the register pairs are written to by the software in the same field. Only a region that contains only single height rows or only double height rows can be scrolled.

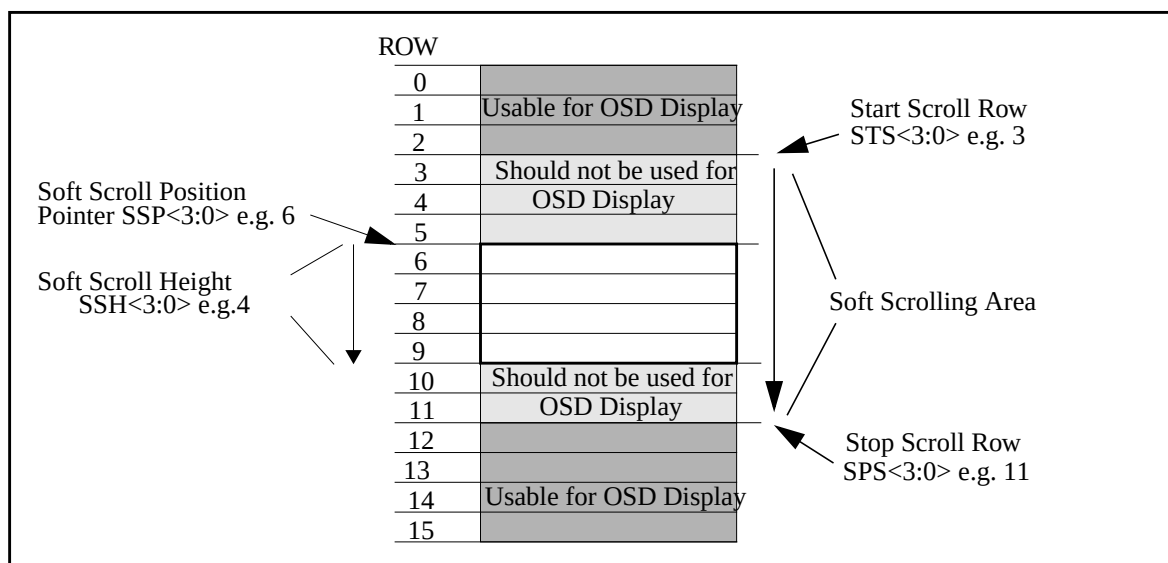


Figure 33 Soft Scroll Area

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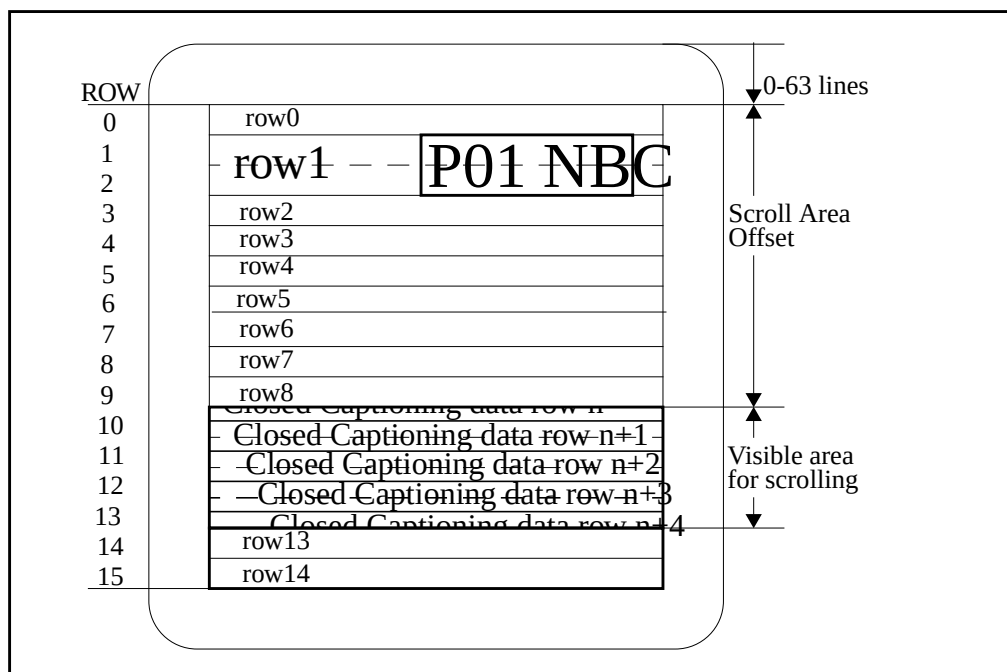


Figure 34 CC Text Areas

TXT:- The display is organised as a fixed size of 25 rows (0 to 24) of 40 columns (0 to 39). This is the standard size for TELETEXT transmissions. The Control Data in row 25 is not displayed but is used to configure the display page correctly.

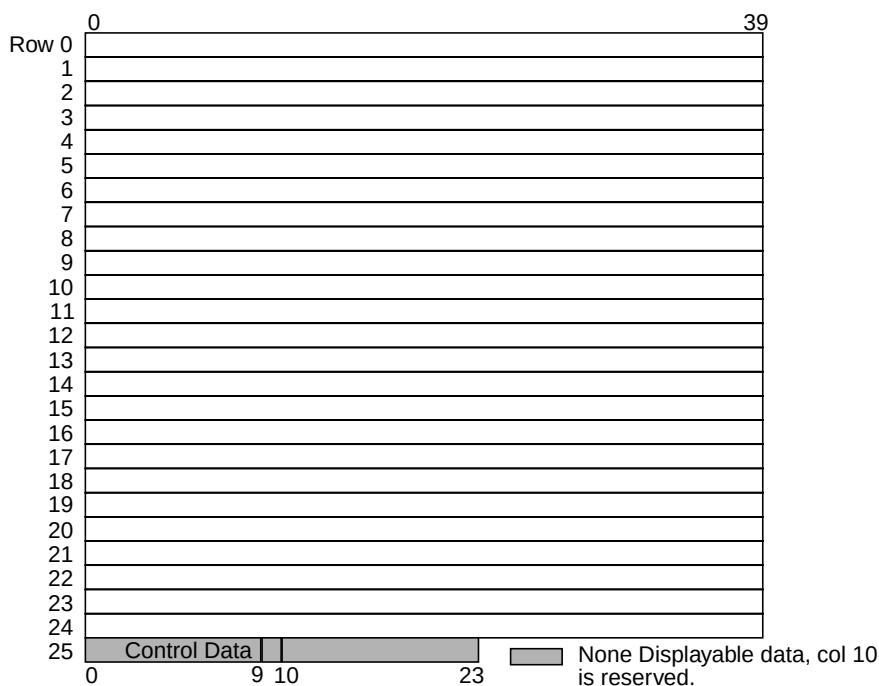


Figure 35 TXT Text Area

TV signal processor-Teletext decoder with
embedded μ -Controller

TDA 935X/6X/8X series

Display Positioning

The display consists of the **Screen Colour** covering the whole screen and the **Text Area** that is placed within the visible screen area. The screen colour extends over a large vertical and horizontal range so that no offset is needed. The text area is offset in both directions relative to the vertical and horizontal sync pulses.

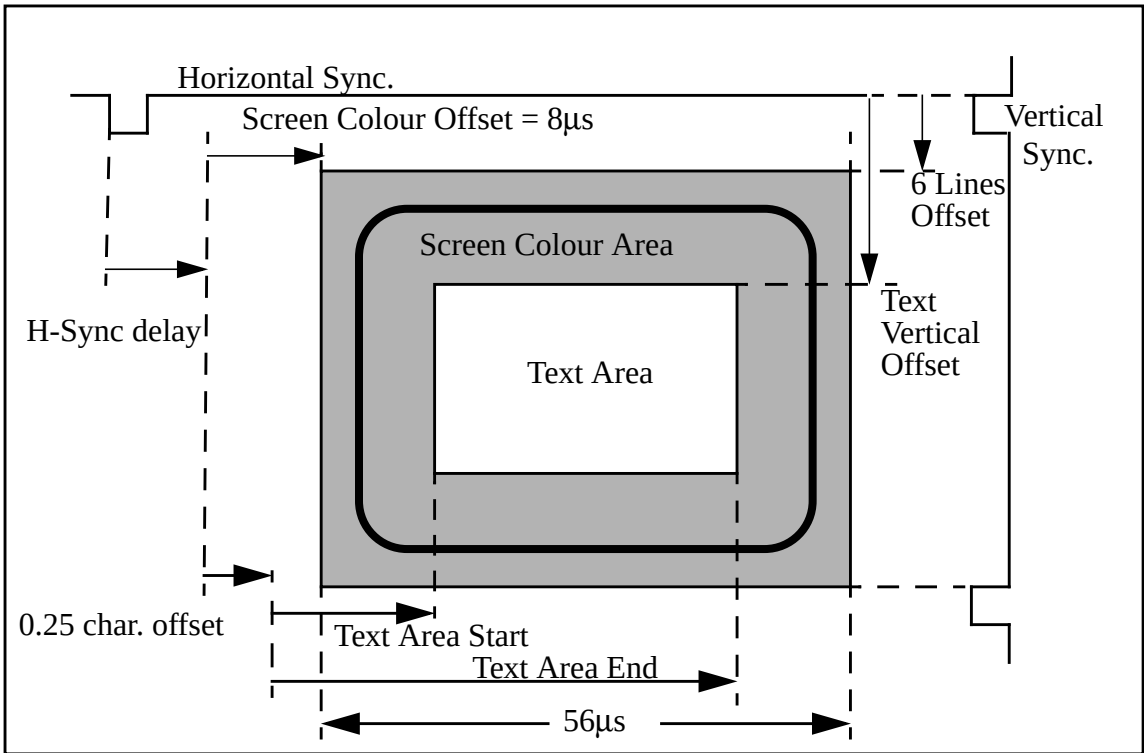


Figure 36 Display Area Positioning

SCREEN COLOUR DISPLAY AREA

This area is covered by the screen colour. The screen colour display area starts with a fixed offset of 8 us from the leading edge of the horizontal sync pulse in the horizontal direction. A vertical offset is not necessary.

Horizontal	start at 8 us after leading edge of H-Sync for 56 us
Vertical	line 9, field 1 (321, field 2) to leading edge of vertical sync (line numbering using 625 Standard)

Table 25 Screen Colour Display Area

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TEXT DISPLAY AREA

The text area can be defined to start with an offset in both the horizontal and vertical direction.

Horizontal	Up to 48 full sized characters per row. Start position setting from 8 to 64 characters from the leading edge of H-Sync. Fine adjustment in quarter characters.
Vertical	256 lines (nominal 41- 297). Start position setting from leading edge of vertical sync, legal values are 4 to 64 lines. (line numbering using 625 Standard)

Table 26 Text Display Area

The horizontal offset is set in the MMR REG2: Text Area Start. The offset is done in full width characters using TAS<5:0> and quarter characters using HOP<1:0> for fine setting. The values 00h to 08h for TAS<5:0> will result in a corrupted display.

The width of the text area is defined in the MMR REG4:Text Area End by setting the end character value TAE<5:0>. This number determines where the background colour of the Text Area will end if set to extend to the end of the row. It will also terminate the character fetch process thus eliminating the necessity of a **row end** attribute. This entails however writing to all positions

The vertical offset is set in the MMR REG1:Text Position Vertical Register. The offset value VOL<5:0> is done in number of TV scan lines.

Note: The Text Position Vertical register should not be set to 00H as the Display Busy interrupt is not generated in these circumstances.

Character Set

To facilitate the global nature of the device the character set has the ability to accommodate a large number of characters, which can be stored in different matrices.

CHARACTER MATRICES

The character matrices that can be accommodated in both display modes are

(H x V x Planes) 12 x 9 x 1, 12 x 10 x 1, 12 x 13 x 1, 12 x 16 x 1. These modes allow two colours character position.

In CC mode two additional character matrices are available to allow four colours per character

(H x V x Planes) 12 x 13 x 2, 12 x 16 x 2.

The characters are stored physically in ROM in a matrix of size either 12 x 10 or 12 x 16.

CHARACTER SET SELECTION

Four character sets are available in the device. A set can consist of alphanumeric characters as required by the WST Teletext or FCC Closed Captioning, Customer definable On-Screen Display characters, and Special Graphic characters.

TV signal processor-Teletext decoder with embedded μ -Controller

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CC:- Only a single character set can be used for display and this is selected using the Basic Set selection TXT18.BS<1:0>. When selecting a character set in CC mode the Twist Set selection TXT19.TS<1:0> should be set to the same value as TXT18.BS<1:0> for correct operation.

TXT:- Two character sets can be displayed at once. These are the basic G0 set or the alternative G0 set (Twist Set). The basic set is selected using TXT18.BS<1:0>, The alternative/twist character set is defined by TXT19.TS<1:0>. Since the alternative character set is an option it can be enabled or disabled using TXT19.TEN, and the language code that is defined for the alternative set is defined by TXT19.TC<2:0>.

The National option table is selected using TXT18.NOT<3:0>, a maximum of 31 National Option tables can be defined when combined with the E/W control bit located in register TXT4.

An example of the character set selection and definitions is show in Table 27.

BS<1:0>/TS<1:0>	Character Set	Example Language
00	Set 0	Latin
01	Set 1	Greek
10	Set 2	Cyrillic
11	Set 3	Closed Caption

Table 27 Character Set Selection

An example of the national option reference table is shown in Table 28. Only a certain number of national options will be relevant for each of the Character Sets.

C12	C13	C14	NOT<3:0>=0000	NOT<3:0>=0001	NOT<3:0>=0010	...	NOT<3:0>=1111
0	0	0	English	Polish	English	...	Polish
0	0	1	German	German	German	...	German
0	1	0	Swedish	Swedish	Swedish	...	Estonian
0	1	1	Italian	Italian	Italian	...	Lettish
1	0	0	French	French	French	...	Russian
1	0	1	Spanish		Spanish	...	Serb-Croat
1	1	0	Czech	Czech	Turkish	...	Czech
1	1	1				...	

Table 28 National Option Selection

**TV signal processor-Teletext decoder with
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TDA 935X/6X/8X seriesCHARACTER SET OPTIONS

A number of pre-defined character sets are available to cover regions throughout the world. These are listed in Table 29.

Name	Matrix (HxV)
Pan European	12 x 10
Cyrillic	12 x 10
Greek/Turkish	12 x 10
Arab/English/French	12 x 10
Thai	12 x 10
Arab/Hebrew	12 x 10
Farsi	12 x 10
Closed Caption	13 x 10

Table 29 Character Set Options

The character set option Pan-European is shown Figure 31 on Page 69.

The Closed Caption character table is shown in Table 30 on Page 80.

ROM ADDRESSING

Three ROMs are used to generate the correct pixel information. The first contains the National option look-up table, the second contains the Basic Character look-up table and the third contains the Character Pixel information.

Although these are individual ROMs, since they do not need to be accessed simultaneously they are all combined into a single ROM unit.

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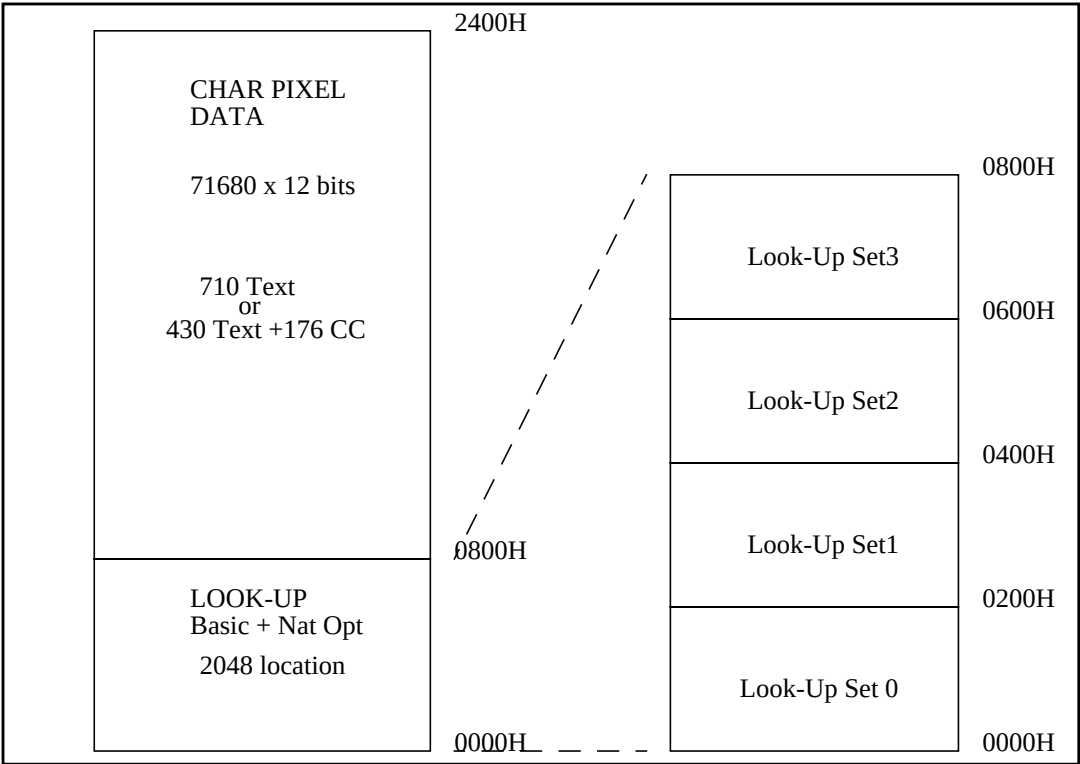


Figure 37 Character ROM Organisation

TV signal processor-Teletext decoder with embedded μ -Controller

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CHARACTER TABLE

CC:- The CC character table is shown in Table 30.

		Character code columns (Bits 4-7)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Character code rows (Bits 0-3)	0		®	SP	0	@	P	ú	p								
	1		°	!	1	A	Q	a	q								
	2		1/2	"	2	B	R	b	r								
	3		¿	#	3	C	S	c	s								
	4		™	\$	4	D	T	d	t								
	5		¢	%	5	E	U	e	u								
	6		£	&	6	F	V	f	v								
	7		♪	'	7	G	W	g	w								
	8		à	(	8	H	X	h	x								
	9		—	)	9	I	Y	i	y								
	A		è	á	:	J	Z	j	z								
	B		â	+	;	K	[	k	ç								
	C		ê	,	<	L	é	l									
	D		î	-	=	M	]	m	ñ								
	E		ô	.	>	N	í	n	ñ								
	F		û	/	?	O	ó	o	n								

Table 30 Closed Caption Character Table

-  Special Characters in column 8 & 9.
-  Additional table locations for normal characters
-  Table locations for normal characters

Redefinable Characters

A number of Dynamically Redefinable Characters (DRC) are available. These are mapped onto the normal character codes, and replace the pre-defined ROM value.

There are 32 DRC's, the first 16 occupy the character codes 80H to 8FH, the second 16 occupy the locations 90H to 9FH. This allows for 32 DRCs or 16 Special DRCs. The re-mapping of the standard OSD to the DRCs is activated when the TXT21.DRCS ENABLE bit is set. The selection of Normal or Special OSD symbols is defined by the TXT21.OSD PLANES.

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Each character is stored in a matrix of 12 x 16 x 1 (V x H x planes), this allows for all possible character matrices to be defined within a single location.

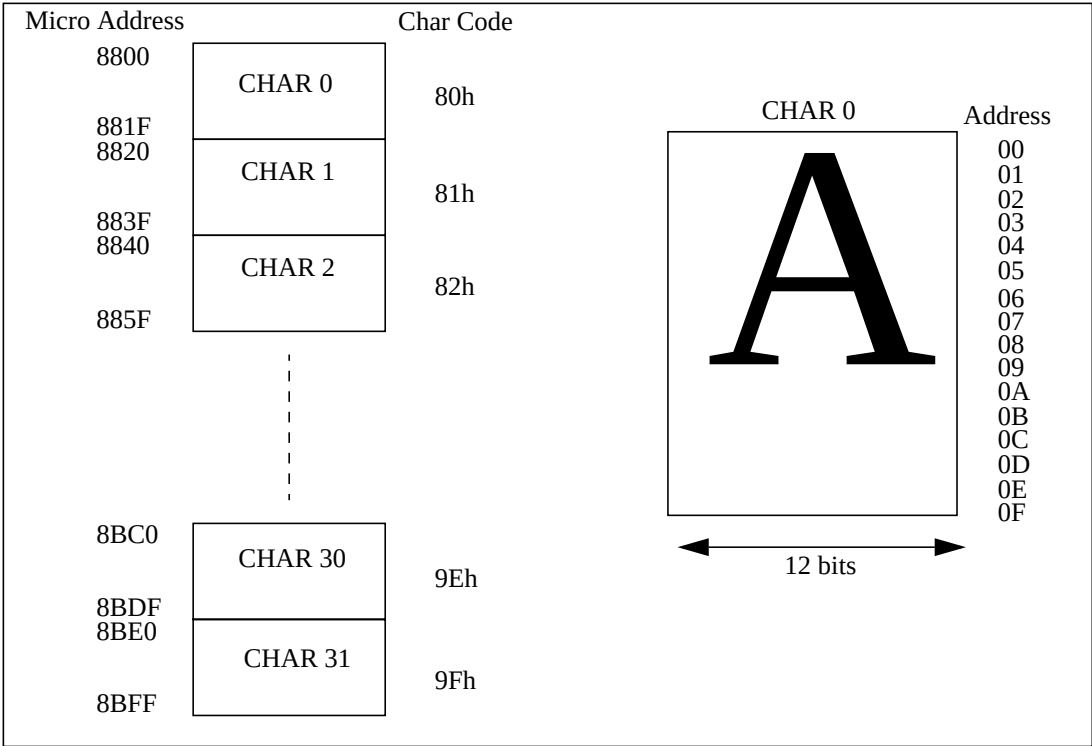


Figure 38 Organisation of DRC RAM

DEFINING CHARACTERS

The DRC RAM is mapped into the 80C51 RAM address space and starts at location 8800H. The character matrix is 12 bits wide and therefore requires two bytes to be written for each word, the first byte (even addresses), addresses the lower 8 bits and the lower nibble of the second byte (odd addresses) addresses the upper 4 bits.

For characters of 9, 10 or 16 lines high the pixel information starts in the first address and continues sequentially for the required number of address.

Characters of 13 lines high are defined with an initial offset of 1 address, this is to allow for correct generation of fringing across boundaries of clustered characters (see Figure 39). The characters continue sequentially for 13 lines after which a further line can again be used for generation of correct fringing across boundaries of clustered characters.

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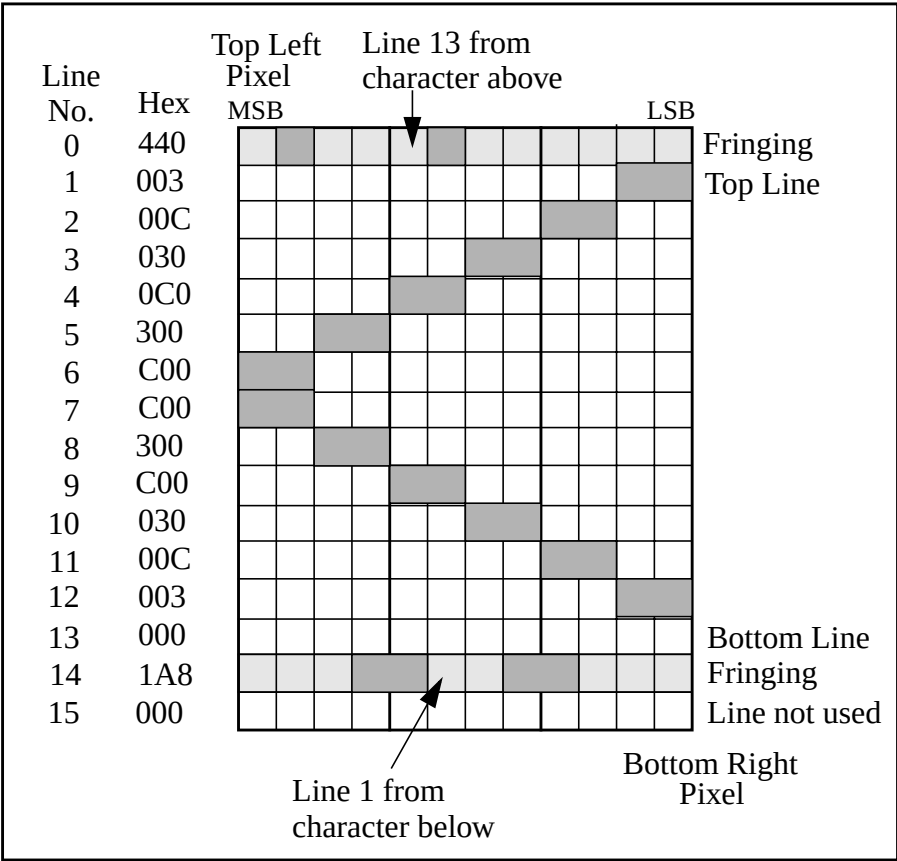


Figure 39 13 Line High DRC's Character Format

RGB BRIGHTNESS CONTROL

A brightness control is provided to allows the RGB upper output voltage level to be modified. The nominal value is 1V into a 150 Ω resistor, but can be varied between 0.7V and 1.2V.

The brightness is set in RGB Brightness register.

BRI3-0	RGB Brightness
0 0 0 0	Lowest value
...	...
1 1 1 1	Highest value

Table 31: RGB Brightness

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Memory Mapped Registers

The memory mapped registers are used to control the display. The registers are mapped into the microcontroller MOVX address space, starting at address 87F0h and extending to 87FF.

MMR ADDRESS SUMMARY

Register No.	Memory Address	Function
0	87F0	Display Control
1	87F1	Text Position Vertical
2	87F2	Text Area Start
3	87F3	Fringing Control
4	87F4	Text Area End
5	87F5	Scroll Area
6	87F6	Scroll Range
7	87F7	RGB Brightness
8	87F8	Status
9	87F9	Reserved
10	87FA	Reserved
11	87FB	Reserved
12	87FC	Reserved
13	87FD	Reserved
14	87FE	Top Scroll Line
15	87FF	Configuration

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MMR MAP

ADD	R/W	Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
87F0	R/W	Display Control	SRC<3>	SRC<2>	SRC<1>	SRC<0>	-	MSH	MOD<1>	MOD<0>
87F1	R/W	Text Position Vertical			VOL<5>	VOL<4>	VOL<3>	VOL<2>	VOL<1>	VOL<0>
87F2	R/W	Text Area Start	HOP<1>	HOP<0>	TAS<5>	TAS<4>	TAS<3>	TAS<2>	TAS<1>	TAS<0>
87F3	R/W	Fringing Control	FRC<3>	FRC<2>	FRC<1>	FRC<0>	FRDN	FRDE	FRDS	FRDW
87F4	R/W	Text Area End	-	-	TAE<5>	TAE<4>	TAE<3>	TAE<2>	TAE<1>	TAE<0>
87F5	R/W	Scroll Area	SSH<3>	SSH<2>	SSH<1>	SSH<0>	SSP<3>	SSP<2>	SSP<1>	SSP<0>
87F6	R/W	Scroll Range	SPS<3>	SPS<2>	SPS<1>	SPS<0>	STS<3>	STS<2>	STS<1>	STS<0>
87F7	R/W	RGB Brightness		-	-	-	BRI<3>	BRI<2>	BRI<1>	BRI<0>
87F8	R	Status read	BUSY	FIELD	SCON	FLR	SCR<3>	SCR<2>	SCR<1>	SCR<0>
87F8	W	Status write	-	-	SCON	FLR	SCR<3>	SCR<2>	SCR<1>	SCR<0>
87FE	R/W	Top Scroll Line	-	-	-	-	SCL<3>	SCL<2>	SCL<1>	SCL<0>
87FF	R/W	Configuration	CC	VDEL<2>	VDEL<1>	VDEL<0>	TXT/V	-	-	-

MMR BIT DEFINITION

Names	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET
Display Control.	SRC<3>	SRC<2>	SRC<1>	SRC<0>	-	MSH	MOD<1>	MOD<0>	00H
SRC<3:0>	Screen Colour definition								
MSH	0 - No meshing of background 1 - Meshing all background colours								
MOD<1:0>	00 - Video 01 - Full Text 10 - Mixed Screen Colour 11 - Mixed Video								
Text Position Vertical			VOL<5>	VOL<4>	VOL<3>	VOL<2>	VOL<1>	VOL<0>	00H
VOL<5:0>	Display start Vertical Offset from V-Sync. (lines)								
Text Area Start	HOP<1>	HOP<0>	TAS<5>	TAS<4>	TAS<3>	TAS<2>	TAS<1>	TAS<0>	00H
HOP<1:0>	Fine Horizontal Offset in quarter of characters								
TAS<5:0>	Text area start								
Fringing Control.	FRC<3>	FRC<2>	FRC<1>	FRC<0>	FRDN	FRDE	FRDS	FRDW	00H
FRC<3:0>	Fringing colour, value address of CLUT								
FRDN	0 - No fringe in North direction 1 - Fringe in North direction								
FRDE	0 - No fringe in East direction 1 - Fringe in East direction								
FRDS	0 - No fringe in South direction 1 - Fringe in South direction								

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FRDW	0 - No fringe in West direction 1 - Fringe in West direction								
Text Area End	-	-	TAE<5>	TAE<4>	TAE<3>	TAE<2>	TAE<1>	TAE<0>	00H
TAE<5:0>	Text Area End, in full characters								
Scroll Area	SSH<3>	SSH<2>	SSH<1>	SSH<0>	SSP<3>	SSP<2>	SSP<1>	SSP<0>	00H
SSH<3:0>	Soft Scroll Height								
SSP<3:0>	Soft Scroll Position								
Scroll Range	SPS<3>	SPS<2>	SPS<1>	SPS<0>	STS<3>	STS<2>	STS<1>	STS<0>	00H
SPS<3:0>	Stop Scroll row								
STS<3:0>	Start Scroll row								
RGB Brightness		-	-	-	BRI<3>	BRI<2>	BRI<1>	BRI<0>	00H
BRI<3:0>	RGB Brightness control								
Status read	BUSY	FIELD	SCON	FLR	SCR<3>	SCR<2>	SCR<1>	SCR<0>	00H
BUSY	0 - Access to display memory will not cause display problems 1 - Access to display memory could cause display problems.								
FIELD	0 - Odd Field 1 - Even Field								
FLR	0 - Active flash region foreground and background displayed 1 - Active flash region background only displayed								
SCR<3:0>	First scroll row								
Status write	-	-	SCON	FLR	SCR<3>	SCR<2>	SCR<1>	SCR<0>	00H
SCON	0 - Scroll area disabled 1 - Scroll area enabled								
FLR	0 - Active flash region foreground and background colour displayed 1 - Active flash region background colour only displayed								
SCR<3:0>	First Scroll Row								
Top Scroll Line	-	-	-	-	SCL<3>	SCL<2>	SCL<1>	SCL<0>	00H
SCL<3:0>	Top line for scroll.								
Configuration	CC	VDEL<2>	VDEL<1>	VDEL<0>	TXT/V	-	-	-	00H
CC	0 - OSD mode 1 - Closed Caption mode								
VDEL<2:0>	Pixel delay between VDS and RGB output 000 - VDS switched to video, not active 001 - VDS active one pixel earlier then RGB 010 - VDS synchronous to RGB 100 - VDS active one pixel after RGB								
TXT/V	BUSY Signal switch 0 - Horizontal 1 - Vertical								

TV signal processor-Teletext decoder with
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References

- [1] 80C51 Based 8-Bit Microcontrollers - Philips Semiconductors (ref. IC20)
- [2] The I2C bus and how to use it (including specification). Philips Semiconductors
- [3] Enhanced Teletext Specification. European Telecommunication Standard ETS 300 706
- [4] World System Teletext and Data Broadcasting System. DTI. December 1987 (525 WST only)
- [5] Specification of the Domestic Video Programme delivery Control System (PDC) EBU Tech. 3262-E
- [6] Recommended Practise for Line 21 data Service EIA-608

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FUNCTIONAL DESCRIPTION OF VIDEO PROCESSOR

Vision IF amplifier

The vision IF amplifier can demodulate signals with positive and negative modulation. The PLL demodulator is completely alignment-free.

The VCO of the PLL circuit is internal and the frequency is fixed to the required value by using the clock frequency of the μ -Controller/Teletext decoder as a reference. The setting of the various frequencies (38, 38.9, 45.75 and 58.75 MHz) can be made via the control bits IFA-IFC in subaddress 27H. Because of the internal VCO the IF circuit has a high immunity to EMC interferences.

QSS Sound circuit (QSS versions)

The sound IF amplifier is similar to the vision IF amplifier and has an external AGC decoupling capacitor.

The single reference QSS mixer is realised by a multiplier. In this multiplier the SIF signal is converted to the intercarrier frequency by mixing it with the regenerated picture carrier from the VCO. The mixer output signal is supplied to the output via a high-pass filter for attenuation of the residual video signals. With this system a high performance hi-fi stereo sound processing can be achieved.

The AM sound demodulator is realised by a multiplier. The modulated sound IF signal is multiplied in phase with the limited SIF signal. The demodulator output signal is supplied to the output via a low-pass filter for attenuation of the carrier harmonics. The AM signal is supplied to the output (pin 44) via the volume control.

It is possible to get the AM output signal (not controlled on amplitude) on the QSS intercarrier output. The selection is made by means of the AM bit in subaddress 29H.

Another possibility is that pin 35 is transferred to external audio input pin and pin 32 to (non-controlled) AM output pin. This can be realised by means of the setting the control bits CMB0 and CMB1 in subaddress 22H.

FM demodulator and audio amplifier (mono versions)

The FM demodulator is realised as narrow-band PLL with external loop filter, which provides the necessary selectivity without using an external band-pass filter. To obtain a good selectivity a linear phase detector and a constant input signal amplitude are required. For this reason the intercarrier signal is internally supplied to the demodulator via a gain controlled amplifier and AGC circuit. The nominal frequency of the demodulator is tuned to the required frequency (4.5/5.5/6.0/6.5 MHz) by means

of a calibration circuit which uses the clock frequency of the μ -Controller/Teletext decoder as a reference. The setting to the wanted frequency is realised by means of the control bits FMA and FMB in control byte 29H.

When required an external sound band-pass filter can be inserted in front of the narrow-band PLL. In that case pin 32 has to be switched to sound IF input by means of the bits SIF (subaddress 21H) and CMB0/CMB1 (subaddress 22H). When the sound IF input is selected the subcarrier output (90° versions) or AVL function (110° versions) are not available.

From the output status bytes it can be read whether the PLL frequency is inside or outside the window and whether the PLL is in lock or not. With this information it is possible to make an automatic search system for the incoming sound frequency. This can be realised by means of a software loop which switches the demodulator to the various frequencies and then select the frequency on which a lock condition has been found.

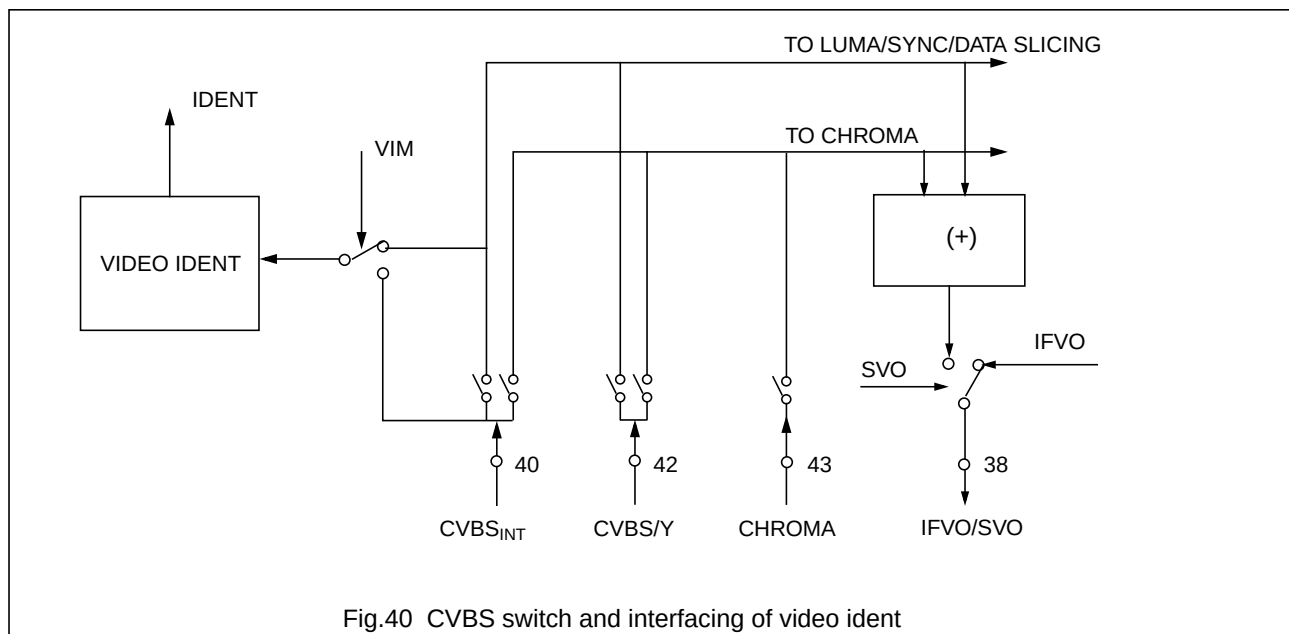
The deemphasis output signal amplitude is independent of the TV standard and has the same value for a frequency deviation of ± 25 kHz at the 4.5 MHz standard and for a deviation of ± 50 Khz for the other standards.

The audio control circuit contains an audio switch and volume control. In the mono intercarrier sound versions the Automatic Volume Levelling (AVL) function can be activated. The pin to which the external capacitor has to be connected depends on the IC version. For the 90° types the capacitor is connected to the EW output pin (pin 20). For the 110° types a choice must be made between the AVL function and a sub-carrier output for comb filter applications. This choice is made via the CBM0 and CMB1bits (in subaddress 22H). When the AVL is active it automatically stabilises the audio output signal to a certain level.

The signal on the deemphasis pin (28) can be supplied to the SCART connector via a buffer stage. It is also possible to use this pin as additional audio input. In that case the internal signal must, of course, be switched off. This can be realised by means of the sound mute bit (SM in subaddress 29H). When the IF circuit is switched to positive modulation the internal signal on the deemphasis pin is automatically muted.

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Video switches

The video switch has one input for an external CVBS or Y/C signal. The switch configuration is given in Fig.40. The selected CVBS signal can be supplied to pin 38, the IF video output. The selection between both signals is realised by means of the SVO bit in subaddress 22H.

The video ident circuit can be connected to the incoming 'internal' video signal or to the selected signal. This ident circuit is independent of the synchronisation and can be used to switch the time-constant of the horizontal PLL depending on the presence of a video signal (via the VID bit). In this way a very stable OSD can be realised.

Because of the availability of the Y/C input and the subcarrier output an external comb-filter can be applied. In that case an external video switch (or comb-filter with integrated switch) must be used.

The subcarrier output is combined with a 3-level output switch (0 V, 4 V and 8 V). The output level and the availability of the subcarrier signal is controlled by the CMB1 and CMB0 bits. The output can be used to switch sound traps etc. It is also possible to use this pin for the connection of the AVL capacitor, external sound IF input or as AM output. The possibilities are illustrated in table 1.

Synchronisation circuit

The IC contains separator circuits for the horizontal and vertical sync pulses and a data-slicing circuit which extracts the digital teletext data from the analog signal.

The horizontal drive signal is obtained from an internal VCO which is running at a frequency of 25 MHz. This oscillator is stabilised to this frequency by using a 12 MHz signal coming from the reference oscillator of the μ -Controller/Teletext decoder.

The horizontal drive is switched on and off via the soft start/stop procedure. This function is realised by means of variation of the T_{ON} of the horizontal drive pulses. In addition the horizontal drive circuit has a 'low-power start-up' function.

The vertical synchronisation is realised by means of a divider circuit. The vertical ramp generator needs an external resistor and capacitor. For the vertical drive a differential output current is available. The outputs must be DC coupled to the vertical output stage.

In the types which are intended for 90° picture tubes the following geometry parameters can be adjusted:

- Horizontal shift
- Vertical amplitude
- Vertical slope
- S-correction
- Vertical shift

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The types which are intended to be used in combination with 110° picture tubes have an East-West control circuit in stead of the AVL function. The additional controls for these types are:

- EW width
- EW parabola width
- EW upper and lower corner parabola correction
- EW trapezium correction
- Vertical zoom

and in some versions:

- horizontal parallelogram and bow correction.

Chroma and luminance processing

The chroma band-pass and trap circuits (including the SECAM cloche filter) are realised by means of gyrators and are tuned to the right frequency by comparing the tuning frequency with the reference frequency of the colour decoder. The luminance delay line and the delay cells for the peaking circuit are also realised with gyrators. The circuit contains a black stretcher function which corrects the black level for incoming signals which have a difference between the black level and the blanking level.

Colour decoder

The ICs can decode PAL, NTSC and SECAM signals. The PAL/NTSC decoder does not need external reference crystals but has an internal clock generator which is stabilised to the required frequency by using the 12 MHz clock signal from the reference oscillator of the μ -Controller/Teletext decoder.

Under bad-signal conditions (e.g. VCR-playback in feature mode), it may occur that the colour killer is activated although the colour PLL is still in lock. When this killing action is not wanted it is possible to overrule the colour killer by forcing the colour decoder to the required standard and to activate the FCO-bit (Forced Colour On) in subaddress 21H.

The Automatic Colour Limiting (ACL) circuit (switchable via the ACL bit in subaddress 20H) prevents that oversaturation occurs when signals with a high chroma-to-burst ratio are received. The ACL circuit is designed such that it only reduces the chroma signal and not the burst signal. This has the advantage that the colour sensitivity is not affected by this function.

The SECAM decoder contains an auto-calibrating PLL demodulator which has two references, viz: the divided 12 MHz reference frequency (obtained from the μ -Controller) which is used to tune the PLL to the desired free-running frequency and the bandgap reference to obtain the correct absolute value of the output signal. The VCO of the PLL is calibrated during each vertical blanking period, when the IC is in search or SECAM mode.

The base-band delay line (TDA 4665 function) is integrated. This delay line is also active during NTSC to obtain a good suppression of cross colour effects. The demodulated colour difference signals are internally supplied to the delay line.

RGB output circuit and black-current stabilization

In the RGB control circuit the signal is controlled on contrast, brightness and saturation. The ICs have a linear input for external RGB signals. It is possible to use this input for the insertion of YUV signals. Switching between RGB and YUV can be realised via the YUV-bit in subaddress 2BH. The signals for OSD and text are internally supplied to the control circuit. The output signal has an amplitude of about 2 Volts black-to-white at nominal input signals and nominal settings of the various controls.

To obtain an accurate biasing of the picture tube the 'Continuous Cathode Calibration' system has been included in these ICs. A black level off set can be made with respect to the level which is generated by the black current stabilization system. In this way different colour temperatures can be obtained for the bright and the dark part of the picture.

The black current stabilization system checks the output level of the 3 channels and indicates whether the black level of the highest output is in a certain window (WBC-bit) or below or above this window (HBC-bit). This indication can be read from the status byte 01 and can be used for automatic adjustment of the V_{g2} voltage during the production of the TV receiver.

During switch-off of the TV receiver a fixed beam current is generated by the black current control circuit. This current ensures that the picture tube capacitance is discharged. During the switch-off period the vertical deflection is placed in an overscan position so that the discharge is not visible on the screen.

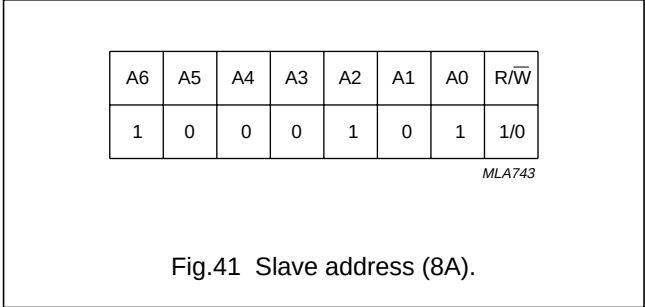
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SOFTWARE CONTROL

The CPU communicates with the peripheral functions using Special function Registers (SFRs) which are addressed as RAM locations. The registers for the Teletext decoder appear as normal SFRs in the μ -Controller memory map and are written to these functions by using a serial bus. This bus is controlled by dedicated hardware which uses a simple handshake system for software synchronisation.

For compatibility reasons and possible re-use of software blocks, the I²C-bus control for the TV processor is organised as in the stand-alone TV signal processors. The TV processor registers cannot be read, so when the content of these registers is needed in the software, a copy should be stored in Auxiliary RAM or Non Volatile RAM. The slave address of the TV signal processor is given in Fig.41.



Valid subaddresses: 06H to 2DH, subaddress FE and FF are reserved for test purposes. Auto-increment mode available for subaddresses.

TV signal processor-Teletext decoder with embedded μ -Controller

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DESCRIPTION OF THE I²C-BUS SUBADDRESSES

Table 32 Inputs TV-processor

FUNCTION	SUBAD (HEX)	DATA BYTE								POR Value
		D7	D6	D5	D4	D3	D2	D1	D0	
Horizontal parallelogram	06	0	0	A5	A4	A3	A2	A1	A0	20
Horizontal bow	07	0	0	A5	A4	A3	A2	A1	A0	20
Hue	08	0	0	A5	A4	A3	A2	A1	A0	00
Horizontal shift (HS)	09	0	0	A5	A4	A3	A2	A1	A0	20
EW width (EW) ⁽¹⁾	0A	0	0	A5	A4	A3	A2	A1	A0	20
EW parabola/width (PW) ⁽¹⁾	0B	0	0	A5	A4	A3	A2	A1	A0	20
EW upper corner parabola ⁽¹⁾	0C	0	0	A5	A4	A3	A2	A1	A0	20
EW lower corner parabola ⁽¹⁾	0D	0	0	A5	A4	A3	A2	A1	A0	20
EW trapezium (TC) ⁽¹⁾	0E	0	0	A5	A4	A3	A2	A1	A0	20
Vertical slope (VS)	0F	0	0	A5	A4	A3	A2	A1	A0	20
Vertical amplitude (VA)	10	0	0	A5	A4	A3	A2	A1	A0	20
S-correction (SC)	11	0	0	A5	A4	A3	A2	A1	A0	20
Vertical shift (VSH)	12	0	0	A5	A4	A3	A2	A1	A0	20
Vertical zoom (VX) ⁽¹⁾	13	0	0	A5	A4	A3	A2	A1	A0	20
Spare	14	0	0	0	0	0	0	0	0	-
Black level off set R/G	15	BLR3	BLR2	BLR1	BLR0	BLG3	BLG2	BLG1	BLG0	88
White point R	16	0	0	A5	A4	A3	A2	A1	A0	20
White point G	17	0	0	A5	A4	A3	A2	A1	A0	20
White point B	18	0	0	A5	A4	A3	A2	A1	A0	20
Peaking	19	0	0	A5	A4	A3	A2	A1	A0	20
Luminance delay time	1A	0	0	0	0	YD3	YD2	YD1	YD0	00
Brightness	1B	0	0	A5	A4	A3	A2	A1	A0	20
Saturation	1C	0	0	A5	A4	A3	A2	A1	A0	20
Contrast	1D	0	0	A5	A4	A3	A2	A1	A0	20
AGC take-over	1E	0	0	A5	A4	A3	A2	A1	A0	20
Volume control	1F	0	0	A5	A4	A3	A2	A1	A0	20
Colour decoder 0	20	CM3	CM2	CM1	CM0	MAT	MUS	ACL	CB	00
Colour decoder 1	21	SIF	0	0	0	0	0	BPS	FCO	00
AV-switch	22	0	0	SVO	CMB1	CMB0	INA	INB	0	00
Spare	23	0	0	0	0	0	0	0	0	-
Synchronisation 0	24	0	HP2	FOA	FOB	POC	STB	VIM	VID	00
Synchronisation 1	25	0	0	FSL	OSO	FORF	FORS	DL	NCIN	00
Deflection	26	0	0	0	0	SBL	VSD	EVG	HCO ⁽¹⁾	00
Vision IF 0	27	IFA	IFB	IFC	VSW	MOD	AFW	IFS	STM	00
Vision IF 1	28	0	0	0	0	0	AGC1	AGC0	FFI	00
Sound	29	BTSC ⁽²⁾	SM1 ⁽²⁾	FMWS ⁽²⁾	AM ⁽³⁾	SM0 ⁽²⁾	AVL ⁽²⁾	FMA ⁽²⁾	FMB ⁽²⁾	00
Control 0	2A	0	IE2	RBL	AKB	CL3	CL2	CL1	CL0	00
Control 1	2B	0	0	0	0	0	0	YUV	HBL ⁽¹⁾	00
Spare	2C	0	0	0	0	0	0	0	0	-
Features 0	2D	0	0	0	0	0	0	0	BKS	00

Note

1. These functions are only available in versions which have the East-West drive output.
2. These bits are only available in the types with FM demodulator. The AVL function is also available in versions with QSS-IF sound which have no East-West output.
3. Only available in types with QSS sound IF circuit and AM demodulator.

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Table 33 Outputs TV-processor

FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Output status bytes	00	POR	IFI	LOCK	SL	CD3	CD2	CD1	CD0
	01	XPR	NDF	FSI	IVW	WBC	HBC	BCF	X
	02	SUP	X	IN2	QSS	AFA	AFB	FMW	FML

Explanation input control data TV-processor

Table 34 Horizontal parallelogram

DAC SETTING	CONTROL
0	screen top 0.5 μ s delayed and screen bottom 0.5 μ s advanced with respect to centre
20	no correction
3F	screen top 0.5 μ s advanced and screen bottom 0.5 μ s delayed with respect to centre

Table 35 Horizontal bow

DAC SETTING	CONTROL
0	screen top and bottom 0.5 μ s delayed with respect to centre
20	no correction
3F	screen top and bottom 0.5 μ s advanced with respect to centre

Table 36 Hue control

DAC SETTING	CONTROL
0	-40°
20	0°
3F	$+40^\circ$

Table 37 Horizontal shift

DAC SETTING	CONTROL
0	-2μ s
20	0
3F	$+2 \mu$ s

Table 38 EW width

DAC SETTING	CONTROL
0	output current 700 μ A
3F	output current 0 μ A

Table 39 EW parabola/width

DAC SETTING	CONTROL
0	output current 0 μ A
3F	output current 440 μ A at top and bottom of screen

Table 40 EW upper/lower corner parabola

DAC SETTING	CONTROL
0	output current 0 μ A
3F	output current -190μ A

Table 41 EW trapezium

DAC SETTING	CONTROL
0	output current at top of screen 100 μ A lower than at bottom
20	no correction
3F	output current at top of screen 100 μ A higher than at bottom

Table 42 Vertical slope

DAC SETTING	CONTROL
0	correction -20%
20	no correction
3F	correction $+20\%$

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Table 43 Vertical amplitude

DAC SETTING	CONTROL
0	amplitude 80%
20	amplitude 100%
3F	amplitude 120%

Table 44 S-correction

DAC SETTING	CONTROL
0	no correction
3F	correction 30%

Table 45 Vertical shift

DAC SETTING	CONTROL
0	shift -5%
20	no correction
3F	shift +5%

Table 46 Vertical zoom

DAC SETTING	CONTROL
0	amplitude 75%
20	amplitude 100%
3F	amplitude 138%

Table 47 Black level off set R/B

DAC SETTING	CONTROL
0	off set of -40 mV
08	no off set
0F	off set of +40 mV

Table 48 White point R/G/B

DAC SETTING	CONTROL
0	gain -3 dB
20	no correction
3F	gain +3 dB

Table 49 Peaking control (overshoot in direction 'black')

DAC SETTING	CONTROL
0	no peaking
20	overshoot 40%
3F	overshoot 80%

Table 50 Y-delay adjustment; note 1

YD0 to YD3	Y-DELAY
YD3	$YD3 \times 160 \text{ ns} +$
YD2	$YD2 \times 80 \text{ ns} +$
YD1	$YD1 \times 40 \text{ ns} +$
YD0	$YD0 \times 40 \text{ ns}$

Note

- For an equal delay of the luminance and chrominance signal the delay must be set at a value of 160 ns. This is only valid for a CVBS signal without group delay distortions.

Table 51 Brightness control

DAC SETTING	CONTROL
0	correction -0.7 V
20	no correction
3F	correction +0.7 V

Table 52 Saturation control

DAC SETTING	CONTROL
0	colour off (-52 dB)
17	saturation nominal
3F	saturation +300%

Table 53 Contrast control

DAC SETTING	CONTROL
0	RGB amplitude -14 dB
20	RGB amplitude nominal
3F	RGB amplitude +6 dB

Table 54 AGC take-over

DAC SETTING	CONTROL
0	tuner take-over at IF input signal of 0.4 mV
3F	tuner take-over at IF input signal of 80 mV

Table 55 Volume control

DAC SETTING	CONTROL
0	attenuation 80 dB
3F	no attenuation

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Table 56 Colour decoder mode, note 1

CM3	CM2	CM1	CM0	DECODER MODE	FREQ
0	0	0	0	PAL/NTSC/SECAM	A
0	0	0	1	PAL/SECAM	A
0	0	1	0	PAL	A
0	0	1	1	NTSC	A
0	1	0	0	SECAM	
0	1	0	1	PAL/NTSC	B
0	1	1	0	PAL	B
0	1	1	1	NTSC	B
1	0	0	0	PAL/NTSC/SECAM	ABCD
1	0	0	1	PAL/NTSC	C
1	0	1	0	PAL	C
1	0	1	1	NTSC	C
1	1	0	0	PAL/NTSC (Tri-Norma)	BCD
1	1	0	1	PAL/NTSC	D
1	1	1	0	PAL	D
1	1	1	1	NTSC	D

Note

- The decoder frequencies for the various standards are obtained from an internal clock generator which is synchronised by a 12 MHz reference signal which is obtained from the μ -Controller clock generator.

These frequencies are:

- A: 4.433619 MHz
- B: 3.582056 MHz (PAL-N)
- C: 3.575611 MHz (PAL-M)
- D: 3.579545 MHz (NTSC-M)

Table 57 PAL-SECAM/NTSC matrix

MAT	MATRIX POSITION
0	adapted to standard
1	PAL matrix

Table 58 NTSC matrix

MUS	MATRIX POSITION
0	Japanese matrix
1	USA matrix

Table 59 Automatic colour limiting

ACL	COLOUR LIMITING
0	not active
1	active

Table 60 Chroma bandpass centre frequency

CB	CENTRE FREQUENCY
0	F_{SC}
1	$1.1 \times F_{SC}$

Table 61 Selection external input for sound IF circuit

SIF	MODE
0	IF input not selected
1	IF input selected (see also table 1)

Table 62 Bypass of chroma base-band delay line

BPS	DELAY LINE MODE
0	active
1	bypassed

Table 63 Forced Colour-On

FCO	CONDITION
0	off
1	on

Table 64 Selected video out (pin 38)

SVO	CONDITION
0	IF video available at output
1	selected CVBS available at output

Table 65 Condition AVL/SNDIF/REFO (pin 32)

CMB1	CMB0	CONDITION
0	0	AVL/SNDIF active; note 1
0	1	output voltage 4 V + subcarrier
1	0	output voltage 0 V
1	1	output voltage 8 V

Note

- The result of this setting depends on the version (FM-PLL or QSS type). The various possibilities are given in table 1.

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Table 66 Source select

INA	INB	SELECTED SIGNALS
0	0	Internal CVBS+ audio
0	1	External CVBS+ audio
1	0	Y/C + ext. audio

Table 67 Synchronization of OSD/TEXT display

HP2	μ -CONTROLLER COUPLED TO
0	ϕ 1 loop
1	ϕ 2 loop

Table 68 Phase 1 (ϕ_1) time constant

FOA	FOB	MODE
0	0	normal
0	1	slow
1	0	slow/fast
1	1	fast

Table 69 Synchronization mode

POC	MODE
0	active
1	not active

Table 70 Stand-by

STB	MODE
0	stand-by
1	normal

Table 71 Video ident mode

VIM	MODE
0	ident coupled to internal CVBS (pin 38)
1	ident coupled to selected CVBS

Table 72 Video ident mode

VID	VIDEO IDENT MODE
0	ϕ 1 loop switched on and off
1	not active

Table 73 Forced slicing level for vertical sync

FSL	SLICING LEVEL
0	slicing level dependent on noise detector
1	fixed slicing level of 70%

Table 74 Switch-off in vertical overscan

OSO	MODE
0	Switch-off undefined
1	Switch-off in vertical overscan

Table 75 Forced field frequency

FORF	FORS	FIELD FREQUENCY
0	0	auto (60 Hz when line not in sync)
0	1	60 Hz
1	0	keep last detected field frequency
1	1	auto (50 Hz when line not in sync)

Table 76 Interlace

DL	STATUS
0	interlace
1	de-interlace

Table 77 Vertical divider mode

NCIN	VERTICAL DIVIDER MODE
0	normal operation
1	switched to search window

Table 78 Service blanking

SBL	SERVICE BLANKING MODE
0	off
1	on

Table 79 Vertical scan disable

VSD	MODE
0	Vertical scan active
1	Vertical scan disabled

Table 80 Enable vertical guard (RGB blanking)

EVG	VERTICAL GUARD MODE
0	not active
1	active

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Table 81 EHT tracking mode

HCO	TRACKING MODE
0	EHT tracking only on vertical
1	EHT tracking on vertical and EW

Table 82 PLL demodulator frequency adjust

IFA	IFB	IFC	IF FREQUENCY
0	0	0	58.75 MHz
0	0	1	45.75 MHz
0	1	0	38.90 MHz
0	1	1	38.00 MHz
1	0	0	33.40 MHz
1	1	0	33.90 MHz

Table 83 Video mute

VSW	STATE
0	normal operation
1	IF-video signal switched off

Table 84 Modulation standard

MOD	MODULATION
0	negative
1	positive

Table 85 AFC window

AFW	AFC WINDOW
0	normal
1	enlarged

Table 86 IF sensitivity

IFS	IF SENSITIVITY
0	normal
1	reduced

Table 87 Search tuning mode

STM	MODE
0	normal operation
1	reduced sensitivity of video indent circuit

Table 88 IF AGC speed

AGC1	AGC0	AGC SPEED
0	0	$0.7 \times \text{norm}$
0	1	norm
1	0	$2 \times \text{norm}$
1	1	$4 \times \text{norm}$

Table 89 Fast filter IF-PLL

FFI	CONDITION
0	normal time constant
1	increased time constant

Table 90 Gain FM demodulator

BTSC	MODE
0	normal operation
1	reduced gain so that BTSC stereo signal remains undistorted

Table 91 Sound mute

SM1	SM0	CONDITION
0	0	see note 1
0	1	see note 2
1	0	mute on
1	1	mute off

Note

1. The mute is activated when the FM-PLL is out-of-lock **or** when the digital acquisition help is out-of-window.
2. The mute is activated when the digital acquisition help is out-of-window.

Table 92 Window selection of Narrow-band sound PLL

FMWS	FUNCTION
0	small window
1	large window

Table 93 Selection QSS out or AM out

AM	MODE
0	QSS output selected
1	AM output selected

TV signal processor-Teletext decoder with embedded μ -Controller

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Table 94 Auto Volume Levelling

AVL	MODE
0	not active
1	active

Table 95 Nominal frequency FM demodulator

FMA	FMB	FREQUENCY
0	0	5.5 MHz
0	1	4.5 MHz
1	0	6.0 MHz
1	1	6.5 MHz

Table 96 Enable fast blanking ext.RGB/YUV

IE2	FAST BLANKING
0	not active
1	active

Table 97 RGB blanking

RBL	RGB BLANKING
0	not active
1	active

Table 98 Black current stabilization

AKB	MODE
0	active
1	not active

Table 99 Cathode drive level (15 steps; 3.5 V/step)

CL3	CL2	CL1	CL0	SETTING CATHODE DRIVE AMPLITUDE; NOTE 1
0	0	0	0	50 V _{BL-WH}
0	1	1	1	75 V _{BL-WH}
1	1	1	1	95 V _{BL-WH}

Note

- The given values are valid for the following conditions:
 - Nominal CVBS input signal
 - Nominal settings for contrast, WPA and peaking
 - Black- and blue-stretch switched-off
 - Gain of output stage such that no clipping occurs
 - Beam current limiting not active
 - The tolerance on these values is about ± 3 V.

Table 100 RGB / YUV switch

YUV	STATUS
0	RGB input activated
1	YUV input activated

Table 101 RGB blanking mode (110° types)

HBL	MODE
0	normal blanking (horizontal flyback)
1	wide blanking

Table 102 Black stretch

BKS	BLACK STRETCH MODE
0	off
1	on

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Explanation output control data TV-processor

Table 103 Power-on-reset

POR	MODE
0	normal
1	power-down

Table 104 Output video identification

IFI	VIDEO SIGNAL
0	no video signal identified
1	video signal identified

Table 105 IF-PLL lock indication

LOCK	INDICATION
0	not locked
1	locked

Table 106 Phase 1 (ϕ_1) lock indication

SL	INDICATION
0	not locked
1	locked

Table 107 Colour decoder mode, note 1

CD3	CD2	CD1	CD0	STANDARD
0	0	0	0	no colour standard identified
0	0	0	1	NTSC with freq. A
0	0	1	0	PAL with freq. A
0	0	1	1	NTSC with freq. B
0	1	0	0	PAL with freq. B
0	1	0	1	NTSC with freq. C
0	1	1	0	PAL with freq. C
0	1	1	1	NTSC with freq. D
1	0	0	0	PAL with freq. D
1	0	1	0	SECAM

Note

1. The values for the various frequencies can be found in the note of table 56.

Table 108 X-ray protection

XPR	OVERVOLTAGE
0	no overvoltage detected
1	overvoltage detected

Table 109 Output vertical guard

NDF	VERTICAL OUTPUT STAGE
0	OK
1	failure

Table 110 Field frequency indication

FSI	FREQUENCY
0	50 Hz
1	60 Hz

Table 111 Condition vertical divider

IVW	STANDARD VIDEO SIGNAL
0	no standard video signal
1	standard video signal (525 or 625 lines)

Table 112 Indication output black level in/out window

WBC	CONDITION
0	black current stabilisation outside window
1	black current stabilisation inside window

Table 113 Indication output black level

HBC	CONDITION
0	black current stabilisation below window
1	black current stabilisation above window

Table 114 Condition black current loop

BCF	CONDITION
0	black current loop is stabilised
1	black current loop is not stabilised

Table 115 Supply voltage indication

SUP	CONDITION
0	supply voltage (8 Volt) not present
1	supply voltage (8 Volt) present

Table 116 Indication RGB input condition

IN2	RGB INSERTION
0	no
1	yes

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Table 117 Version indication

QSS	IC VERSION
0	version with intercarrier mono sound circuit
1	version with QSS-IF circuit

Table 118 AFC output

AFA	AFB	CONDITION
0	0	outside window; RF too low
0	1	outside window; RF too high
1	0	in window; below reference
1	1	in window; above reference

Table 119 Indication FM-PLL in/out window

FMW	CONDITION
0	FM-PLL in window
1	FM-PLL out of window

Table 120 Indication FM-PLL in/out lock

FML	CONDITION
0	FM-PLL out of lock
1	FM-PLL locked

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	9.0	V
V_{DD}	supply voltage (all digital supplies)		–0.5	5.0	V
V_I	digital inputs	note 1	–0.5	$V_{DD} + 0.5$	V
V_O	digital outputs	note 1	–0.5	$V_{DD} + 0.5$	V
I_O	output current (each output)		–	± 10	mA
I_{IOK}	DC input or output diode current		–	± 20	mA
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
T_{sol}	soldering temperature	for 5 s	–	260	°C
T_j	operating junction temperature		–	150	°C
V_{es}	electrostatic handling	HBM; all pins; notes 2 and 3	–2000	+2000	V
		MM; all pins; notes 2 and 4	–300	+300	V

Notes

1. This maximum value has an absolute maximum of 5.5 V independent of V_{DD} .
2. All pins are protected against ESD by means of internal clamping diodes.
3. Human Body Model (HBM): $R = 1.5 \text{ k}\Omega$; $C = 100 \text{ pF}$.
4. Machine Model (MM): $R = 0 \text{ }\Omega$; $C = 200 \text{ pF}$.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th \text{ j-a}}$	thermal resistance from junction to ambient in free air	40	K/W

QUALITY SPECIFICATION

In accordance with “SNW-FQ-611E”.

Latch-up

At an ambient temperature of 70 °C all pins meet the following specification:

- $I_{trigger} \geq 100 \text{ mA}$ or $\geq 1.5V_{DD(max)}$
- $I_{trigger} \leq -100 \text{ mA}$ or $\leq -0.5V_{DD(max)}$.

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CHARACTERISTICS OF MICRO-COMPUTER AND TEXT DECODER

$V_{DD} = 3.3 \text{ V} \pm 10\%$; $V_{SS} = 0 \text{ V}$; $T_{amb} = -20 \text{ to } +70 \text{ }^{\circ}\text{C}$; unless otherwise specified

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
VM.1.1	supply voltage ($V_{DDA/P/C}$)		3.0	3.3	3.6	V
VM.1.2	periphery supply current (I_{DDP})	note 1	1	–	–	mA
VM.1.3	core supply current (I_{DDC})		–	15	tbf	mA
VM.1.4	analog supply current (I_{DDA})		–	45	tbf	mA
Digital inputs						
RESET						
I.1.1	low level input voltage		–	–	0.8	V
I.1.2	high level input voltage		2.0	–	5.5	V
I.1.3	hysteresis of Schmitt Trigger input		0.4	–	0.7	V
I.1.4	input leakage current	$V_I = 0$	–	–	1	μA
I.1.5	equivalent pull down resistance	$V = V_{DD}$	–	33	–	$\text{k}\Omega$
I.1.6	capacitance of input pin		–	–	10	pF
Digital input/outputs						
P1.0 TO P1.3, P2.0 AND P3.0 TO P3.3						
IO.1.1	low level input voltage		–	–	0.8	V
IO.1.2	high level input voltage		2.0	–	5.5	V
IO.1.3	hysteresis of Schmitt Trigger input		0.4	–	0.7	V
IO.1.4	low level output voltage	$I_{OL} = 4 \text{ mA}$	–	–	0.4	V
IO.1.5	high level output voltage	open drain	–	–	5.5	V
IO.1.6	high level output voltage	$I_{OH} = 4 \text{ mA}$	2.4	–	–	V
IO.1.7	output rise time (push-pull only) 10% to 90%	load 100 pF	–	16	–	ns
IO.1.8	output fall time 10% to 90%	load 100pF	–	14	–	ns
IO.1.9	load capacitance		–	–	100	pF
IO.1.10	capacitance of input pin		–	–	10	pF

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P0.5 AND P0.6						
IO.2.1	low level input voltage		–	–	0.8	V
IO.2.2	high level input voltage		2.0	–	5.5	V
IO.2.3	hysteresis of Schmitt Trigger input		0.4	–	0.7	V
IO.2.4	low level output voltage	$I_{OL} = 8\text{mA}$	–	–	0.4	V
IO.2.5	high level output voltage	open drain	–	–	5.5	V
IO.2.6	high level output voltage	$I_{OH} = 8\text{mA}$	2.4	–	–	V
IO.2.7	output rise time (push-pull only) 10% to 90%	load 100 pF	–	16	–	ns
IO.2.8	output fall time 10% to 90%	load 100pF	–	14	–	ns
IO.2.9	load capacitance		–	–	100	pF
IO.2.10	capacitance of input pin		–	–	10	pF
P1.6 AND P1.7						
IO.3.1	low level input voltage (V_{IL})		–	–	1.5	V
IO.3.2	high level input voltage (V_{IH})		3.0	–	5.5	V
IO.3.3	hysteresis of Schmitt-trigger input		0.2	–	–	V
IO.3.4	low level output voltage	sink current 8mA	0	–	0.4	V
IO.3.5	high level output voltage	open drain	–	–	5.5	V
IO.3.6	output fall time (V_{IH} to V_{IL} for C_L)		$20+0.1 \times C_L$	–	250	ns
IO.3.7	bus load capacitance		10	–	400	pF
IO.3.8	capacitance of IO pin		–	–	10	pF
Crystal oscillator						
OSCIN; NOTE 2						
X.1.1	resonator frequency		–	12	–	MHz
X.1.2	input capacitance (C_i)		–	4.1	–	pF
X.1.3	output capacitance (C_o)		–	2.9	–	pF
X.1.4	$C_{x1} = C_{x2}$		12	–	56	pF
X.1.5	R_i (crystal)		–	–	100	Ω

Note

- Peripheral current is dependent on external components and voltage levels on I/Os
- The simplified circuit diagram of the oscillator is given in Fig.42.

A suitable crystal for this oscillator is the Saronix type 9922 520 00169. The nominal tuning of the crystal is important to obtain a symmetrical catching range for the PLL in the colour decoder. This tuning can be adapted by means of the values of the capacitors C_{x1} and C_{x2} in Fig.42. Good results were obtained with capacitor values of 39 pF, however, for a new application the optimum value should be determined by checking the symmetry of the catching range of the colour decoder.

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CHARACTERISTICS OF TV-PROCESSORS

$V_P = 8\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
MAIN SUPPLY; NOTE 1						
V.1.1	supply voltage		7.2	8.0	8.8	V
V.1.2	supply current main supply		–	tbf	–	mA
V.1.3	supply current 2 nd supply		–	tbf	–	mA
V.1.4	total power dissipation		–	tbf	–	mW
IF circuit						
VISION IF AMPLIFIER INPUTS						
M.1.1	input sensitivity (RMS value)	note 2 $f_i = 38.90\text{ MHz}$	–	35	100	μV
M.1.2		$f_i = 45.75\text{ MHz}$	–	35	100	μV
M.1.3		$f_i = 58.75\text{ MHz}$	–	35	100	μV
M.1.4	input resistance (differential)	note 3	–	2	–	k Ω
M.1.5	input capacitance (differential)	note 3	–	3	–	pF
M.1.6	gain control range		64	–	–	dB
M.1.7	maximum input signal (RMS value)		150	–	–	mV
PLL DEMODULATOR; NOTES 4 AND 5						
M.2.1	Free-running frequency of VCO	PLL not locked, deviation from nominal setting	–500	–	+500	kHz
M.2.2	Catching range PLL	without SAW filter	–	± 1	–	MHz
M.2.3	delay time of identification	via LOCK bit	–	–	20	ms
VIDEO AMPLIFIER OUTPUT (PIN 38); NOTES 7 AND 8						
M.3.1	zero signal output level	negative modulation; note 9	–	4.7	–	V
M.3.2		positive modulation; note 9	–	2.0	–	V
M.3.3	top sync level	negative modulation	1.9	2.0	2.1	V
M.3.4	white level	positive modulation	–	4.5	–	V
M.3.5	difference in amplitude between negative and positive modulation		–	0	15	%
M.3.6	video output impedance		–	50	–	Ω
M.3.7	internal bias current of NPN emitter follower output transistor		1.0	–	–	mA
M.3.8	maximum source current		–	–	5	mA
M.3.9	bandwidth of demodulated output signal	at –3 dB	6	9	–	MHz
M.3.10	differential gain	note 10	–	2	5	%
M.3.11	differential phase	notes 10 and 6	–	–	5	deg

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIDEO AMPLIFIER (CONTINUED)						
M.3.12	video non-linearity	note 11	–	–	5	%
M.3.13	white spot clamp level		–	5.3	–	V
M.3.14	noise inverter clamping level	note 12	–	1.7	–	V
M.3.15	noise inverter insertion level (identical to black level)	note 12	–	2.8	–	V
M.3.16	intermodulation blue	notes 6 $V_o = 0.92$ or 1.1 MHz	60	66	–	dB
M.3.17		$V_o = 2.66$ or 3.3 MHz	60	66	–	dB
M.3.18	yellow	$V_o = 0.92$ or 1.1 MHz	56	62	–	dB
M.3.19		$V_o = 2.66$ or 3.3 MHz	60	66	–	dB
M.3.20	signal-to-noise ratio	notes 6 and 13 weighted	56	60	–	dB
M.3.21		unweighted	49	53	–	dB
M.3.22	residual carrier signal	note 6	–	5.5	–	mV
M.3.23	residual 2nd harmonic of carrier signal	note 6	–	2.5	–	mV
IF AND TUNER AGC; NOTE 14						
Timing of IF-AGC						
M.4.1	modulated video interference	30% AM for 1 mV to 100 mV; 0 to 200 Hz (system B/G)	–	–	10	%
M.4.2	response time to IF input signal amplitude increase of 52 dB	positive and negative modulation	–	2	–	ms
M.4.3	response to an IF input signal	negative modulation	–	50	–	ms
M.4.4	amplitude decrease of 52 dB	positive modulation	–	100	–	ms
Tuner take-over adjustment (via I ² C-bus)						
M.5.1	minimum starting level for tuner take-over (RMS value)		–	0.4	0.8	mV
M.5.2	maximum starting level for tuner take-over (RMS value)		75	150	–	mV
Tuner control output						
M.6.1	maximum tuner AGC output voltage	maximum tuner gain; note 3	–	–	9	V
M.6.2	output saturation voltage	minimum tuner gain; $I_o = 2$ mA	–	–	300	mV
M.6.3	maximum tuner AGC output swing		5	–	–	mA
M.6.4	leakage current RF AGC		–	–	1	μ A
M.6.5	input signal variation for complete tuner control		0.5	2	4	dB

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AFC OUTPUT (VIA I ² C-BUS); NOTE 15						
M.7.1	AFC resolution		–	2	–	bits
M.7.2	window sensitivity		–	125	–	kHz
M.7.3	window sensitivity in large window mode		–	275	–	kHz
VIDEO IDENTIFICATION OUTPUT (VIA IFI BIT IN OUTPUT BYTE 00)						
M.8.1	delay time of identification after the AGC has stabilized on a new transmitter		–	–	10	ms
QSS Sound IF circuit (in versions with QSS demodulation)						
SOUND IF AMPLIFIER						
Q.1.1	input sensitivity (RMS value)	FM mode (–3 dB)	–	30	70	μ V
Q.1.2		AM mode (–3 dB)	–	60	100	μ V
Q.1.3	maximum input signal (RMS value)	FM mode	50	70	–	mV
Q.1.4		AM mode	80	140	–	mV
Q.1.5	input resistance (differential)	note 3	–	2	–	k Ω
Q.1.6	input capacitance (differential)	note 3	–	3	–	pF
Q.1.7	gain control range		64	–	–	dB
Q.1.8	crosstalk attenuation between SIF and VIF input		50	–	–	dB
SOUND IF INTERCARRIER OUTPUT; PIN 32 WITH AM = 0						
Q.2.1	output signal amplitude (RMS value)	SC-1; sound carrier 2 off	75	100	125	mV
Q.2.2	bandwidth (-3 dB)		7.5	9	–	MHz
Q.2.3	residual IF sound carrier (RMS value)		–	2	–	mV
Q.2.4	output resistance		–	tbf	–	Ω
Q.2.5	DC output voltage		–	tbf	–	V
Q.2.6	internal bias current of emitter follower		–	tbf	–	mA
Q.2.7	maximum AC and DC sink current		–	tbf	–	mA
Q.2.8	maximum AC and DC source current		–	tbf	–	mA

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SOUND INTERCARRIER OUTPUT (CONTINUED)						
Q.2.9	weighted S/N ratio (SC1/SC2). Ratio of PC/SC1 at vision IF input of 40 dB or higher, note 16	black picture	53/48	58/55	–	dB
Q.2.10		white picture	52/47	55/53	–	dB
Q.2.11		6 kHz sinewave (black-to-white modulation)	44/42	48/46	–	dB
Q.2.12		250 kHz sine wave (black-to-white modulation)	44/25	48/30	–	dB
Q.2.13		sound carrier subharmonics (f=2.75 MHz ± 3 kHz)	45/44	51/50	–	dB
Q.2.14		sound carrier subharmonics (f=2.87 MHz ± 3 kHz)	46/45	52/51	–	dB
AM SOUND OUTPUT; PIN 32 OR 35 DEPENDING ON SETTING OF CMB0/CMB1 AND AM BITS (SEE TABLE 1)						
Q.3.1	AF output signal amplitude (RMS value)	54% modulation	400	500	600	mV
Q.3.2	total harmonic distortion	54% modulation	–	0.5	1.0	%
Q.3.21	total harmonic distortion	80% modulation	–	tbf	5.0	%
Q.3.3	AF bandwidth	–3 dB	100	125	–	kHz
Q.3.4	weighted signal-to-noise ratio		47	53	–	dB
Q.3.5	DC output voltage		–	tbf	–	V
Q.3.6	power supply ripple rejection		–	tbf	–	dB

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM demodulator and audio amplifier (in versions with mono intercarrier sound channel)						
FM-PLL DEMODULATOR; NOTE 17						
G.1.1	IF intercarrier level at IF video output (RMS value) for lock-in of PLL		–	–	tbf	mV
G.1.2	gain control range AGC amplifier		26	30	–	dB
G.1.3	catching range PLL	note 18	–	± 225	–	kHz
G.1.4	maximum phase detector output current		–	± 100	–	μ A
G.1.5	VCO steepness $\Delta f_{FM}/\Delta V_C$ (K_0)		–	3.3	–	MHz/V
G.1.6	phase detector steepness $\Delta I_C/\Delta \phi_{VFM}$ (K_D)		–	9	–	μ A/rad
G.1.7	AM rejection	note 19	40	46	–	dB
EXTERNAL SOUND IF INPUT (PIN 32, WHEN SELECTED; SEE ALSO TABLE 1)						
G.1.8	input limiting for lock-in of PLL (RMS value)		–	1	2	mV
G.1.9	input resistance	note 3	–	8.5	–	k Ω
G.1.10	input capacitance	note 3	–	–	5	pF
DE-EMPHASIS OUTPUT (PIN 28); NOTE 21						
G.2.1	output signal amplitude (RMS value)	note 18	–	500	–	mV
G.2.2	output resistance		–	15	–	k Ω
G.2.3	DC output voltage		–	3	–	V
AUDIO INPUT VIA PIN 28; NOTE 21						
G.2.4	input signal amplitude (RMS value)		–	500	–	mV
G.2.5	input resistance		–	15	–	k Ω
G.2.6	voltage gain between input and output	maximum volume	–	9	–	dB

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio Amplifier						
AUDIO OUTPUT (FM VERSIONS) OR VOLUME CONTROLLED AM-OUT (QSS VERSIONS)						
A.1.1	controlled output signal amplitude (RMS value)	-6 dB; note 18	500	700	900	mV
A.1.2	output resistance		–	500	–	Ω
A.1.3	DC output voltage		–	3.0	–	V
A.1.4	total harmonic distortion	note 22	–	–	0.5	%
A.1.5	total harmonic distortion	note 23	–	–	tbf	%
A.1.6	power supply rejection	note 6	–	tbf	–	dB
A.1.7	internal signal-to-noise ratio	note 6 + 24	–	60	–	dB
A.1.8	external signal-to-noise ratio	note 6 + 24	–	80	–	dB
A.1.9	output level variation with temperature	note 6 + 25	–	–	tbf	dB
A.1.10	control range	see also Fig.43	–	80	–	dB
A.1.11	suppression of output signal when mute is active		–	80	–	dB
A.1.12	DC shift of the output when mute is active		–	10	50	mV
EXTERNAL AUDIO INPUT						
A.2.1	input signal amplitude (RMS value)		–	500	2000	mV
A.2.2	input resistance		–	25	–	k Ω
A.2.3	voltage gain between input and output	maximum volume	–	9	–	dB
A.2.4	crosstalk between internal and external audio signals		60	–	–	dB
AUTOMATIC VOLUME LEVELLING; NOTE 26						
A.3.1	gain at maximum boost		–	6	–	dB
A.3.2	gain at minimum boost		–	-14	–	dB
A.3.3	charge (attack) current		–	1	–	mA
A.3.4	discharge (decay) current		–	200	–	nA
A.3.5	control voltage at maximum boost		–	1	–	V
A.3.6	control voltage at minimum boost		–	5	–	V

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CVBS, Y/C, RGB, CD AND LUMINANCE OUT- AND INPUTS						
CVBS-Y/C SWITCH						
S.1.1	CVBS or Y input voltage (peak-to-peak value)	note 27	–	1.0	1.4	V
S.1.2	CVBS or Y input current		–	4	–	μ A
S.1.3	suppression of non-selected CVBS input signal	notes 6 and 28	50	–	–	dB
S.1.4	chrominance input voltage (burst amplitude)	note 3 and 29	–	0.3	1.0	V
S.1.5	chrominance input impedance		–	50	–	k Ω
CVBS OUTPUT ON PIN 38 (WHEN ACTIVATED, NOTE 8)						
S.1.9	output signal amplitude (peak-to-peak value)		–	2.0	–	V
S.1.10	top sync level		–	1.8	–	V
S.1.11	output impedance		–	–	50	Ω
EXTERNAL RGB / YUV INPUT						
S.2.1	RGB input signal amplitude for an output signal of 2 V (black-to-white) (peak-to-peak value)	note 30	–	0.7	0.8	V
S.2.2	RGB input signal amplitude before clipping occurs (peak-to-peak value)	note 6	1.0	–	–	V
S.2.3	Y input signal amplitude (peak-to-peak value)	input signal amplitude for an output signal of 2 V (black-to-white); YUV bit active; note 31	–	1.4	2.0	V
S.2.4	U input signal amplitude (peak-to-peak value)		–	1.33	2.0	V
S.2.5	V input signal amplitude (peak-to-peak value)		–	1.05	1.5	V
S.2.6	difference between black level of internal and external signals at the outputs		–	–	20	mV
S.2.7	input currents	no clamping; note 3	–	0.1	1	μ A
S.2.8	delay difference for the three channels	note 6	–	0	20	ns

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FAST BLANKING						
S.3.1	input voltage	no data insertion	–	–	0.4	V
S.3.2		data insertion	0.9	–	–	V
S.3.3	maximum input pulse	insertion	–	–	3.0	V
S.3.4	delay time from RGB in to RGB out	data insertion; note 6	–	–	tbf	ns
S.3.5	delay difference between insertion to RGB out and RGB in to RGB out	data insertion; note 6	–	–	tbf	ns
S.3.6	input current		–	–	0.2	mA
S.3.7	suppression of internal RGB signals	notes 6 and 28; insertion; $f_i = 0$ to 5 MHz	–	55	–	dB
S.3.8	suppression of external RGB signals	notes 6 and 28; no insertion; $f_i = 0$ to 5 MHz	–	55	–	dB
Chrominance filters						
CHROMINANCE TRAP CIRCUIT; NOTE 32						
F.1.1	trap frequency		–	f_{osc}	–	MHz
F.1.2	Bandwidth at $f_{SC} = 3.58$ MHz	–3 dB	–	2.8	–	MHz
F.1.3	Bandwidth at $f_{SC} = 4.43$ MHz	–3 dB	–	3.4	–	MHz
F.1.4	colour subcarrier rejection		24	26	–	dB
F.1.5	trap frequency during SECAM reception		–	4.3	–	MHz
CHROMINANCE BANDPASS CIRCUIT						
F.2.1	centre frequency (CB = 0)		–	f_{osc}	–	MHz
F.2.2	centre frequency (CB = 1)		–	$1.1 \times f_{osc}$	–	MHz
F.2.3	bandpass quality factor		–	3	–	
CLOCHE FILTER						
F.3.1	centre frequency		4.26	4.29	4.31	MHz
F.3.2	Bandwidth		241	268	295	kHz

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Luminance Processing						
Y DELAY LINE						
F.4.1	delay time	note 6	–	480	–	ns
F.4.2	tuning range delay time	8 steps	–160	–	+160	ns
F.4.3	bandwidth of internal delay line	note 6	8	–	–	MHz
PEAKING CONTROL; NOTE 33						
F.5.1	width of preshoot or overshoot	note 3	–	160	–	ns
F.5.2	peaking signal compression threshold		–	50	–	IRE
F.5.3	overshoot at maximum peaking	positive	–	45	–	%
F.5.4		negative	–	80	–	%
F.5.5	Ratio negative/positive overshoot		–	1.8	–	
F.5.6	peaking control curve	63 steps	see Fig.44			
BLACK LEVEL STRETCHER; NOTE 34						
F.7.1	Maximum black level shift		15	21	27	IRE
F.7.2	level shift at 100% peak white		–1	0	1	IRE
F.7.3	level shift at 50% peak white		–1	–	3	IRE
F.7.4	level shift at 15% peak white		6	8	10	IRE

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal and vertical synchronization and drive circuits						
SYNC VIDEO INPUT						
H.1.1	sync pulse amplitude	note 3	50	300	350	mV
H.1.2	slicing level for horizontal sync	note 35	–	50	–	%
H.1.3	slicing level for vertical sync	note 35	–	30	–	%
HORIZONTAL OSCILLATOR						
H.2.1	free running frequency		–	15625	–	Hz
H.2.2	spread on free running frequency		–	–	± 2	%
H.2.3	frequency variation with respect to the supply voltage	$V_P = 8.0\text{ V} \pm 10\%$; note 6	–	0.2	0.5	%
H.2.4	frequency variation with temperature	$T_{\text{amb}} = 0\text{ to }70\text{ }^{\circ}\text{C}$; note 6	–	–	80	Hz
FIRST CONTROL LOOP; NOTE 36						
H.3.1	holding range PLL		–	± 0.9	± 1.2	kHz
H.3.2	catching range PLL	note 6	± 0.6	± 0.9	–	kHz
H.3.3	signal-to-noise ratio of the video input signal at which the time constant is switched		–	20	–	dB
H.3.4	hysteresis at the switching point		–	3	–	dB
SECOND CONTROL LOOP						
H.4.1	control sensitivity		–	150	–	$\mu\text{s}/\mu\text{s}$
H.4.2	control range from start of horizontal output to flyback at nominal shift position		–	19	–	μs
H.4.3	horizontal shift range	63 steps	± 2	–	–	μs
H.4.4	control sensitivity for dynamic compensation		–	7.6	–	$\mu\text{s}/\text{V}$
H.4.5	Voltage to switch-on the 'flash' protection	note 37	6	–	–	V
H.4.6	Input current during protection		–	–	1	mA
H.4.7	control range of the parallelogram correction	note 38	–	± 0.5	–	μs
H.4.8	control range of the bow correction	note 38	–	± 0.5	–	μs

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HORIZONTAL OUTPUT; NOTE 39						
H.5.1	LOW level output voltage	$I_O = 10 \text{ mA}$	–	–	0.3	V
H.5.2	maximum allowed output current		10	–	–	mA
H.5.3	maximum allowed output voltage		–	–	V_P	V
H.5.4	duty factor	$V_{OUT} = \text{LOW} (T_{ON})$	–	55	–	%
H.5.5	switch-on time of horizontal drive pulse		–	100	–	ms
H.5.6	switch-off time of horizontal drive pulse		–	43	–	ms
FLYBACK PULSE INPUT AND SANDCASTLE OUTPUT						
H.6.1	required input current during flyback pulse	note 3	100	–	300	μA
H.6.2	output voltage	during burst key	4.8	5.3	5.8	V
		during blanking	1.8	2.0	2.2	V
H.6.3	clamped input voltage during flyback		2.6	3.0	3.4	V
H.6.4	pulse width	burst key pulse	3.3	3.5	3.7	μs
H.6.5		vertical blanking, note 40	–	14	–	lines
H.6.6	delay of start of burst key to start of sync		4.6	4.8	5.0	μs
VERTICAL OSCILLATOR; NOTE 41						
H.7.1	free running frequency		–	50/60	–	Hz
H.7.2	locking range		45	–	64.5/72	Hz
H.7.3	divider value not locked		–	625/525	–	lines
H.7.4	locking range		434/488	–	722	lines/ frame
VERTICAL RAMP GENERATOR						
H.8.1	sawtooth amplitude (peak-to-peak value)	$V_S = 1\text{FH}$; $C = 100 \text{ nF}$; $R = 39 \text{ k}\Omega$	–	3.0	–	V
H.8.2	discharge current		–	1	–	mA
H.8.3	charge current set by external resistor	note 42	–	16	–	μA
H.8.4	vertical slope	control range (63 steps)	–20	–	+20	%
H.8.5	charge current increase	$f = 60 \text{ Hz}$	–	19	–	%
H.8.6	LOW level of ramp		–	2.3	–	V
VERTICAL DRIVE OUTPUTS						
H.9.1	differential output current (peak-to-peak value)	$V_A = 1\text{FH}$	–	0.95	–	mA
H.9.2	common mode current		–	400	–	μA
H.9.3	output voltage range		0	–	4.0	V

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EHT TRACKING/OVERVOLTAGE PROTECTION						
H.10.1	input voltage		1.2	–	2.8	V
H.10.2	scan modulation range		–5	–	+5	%
H.10.3	vertical sensitivity		–	6.3	–	%/V
H.10.4	EW sensitivity	when switched-on	–	–6.3	–	%/V
H.10.5	EW equivalent output current		+100	–	–100	μ A
H.10.6	overvoltage detection level	note 37	–	3.9	–	V
DE-INTERLACE						
H.11.1	first field delay		–	0.5H	–	
EW WIDTH; NOTE 43						
H.12.1	control range	63 steps	100	–	65	%
H.12.2	equivalent output current		0	–	700	μ A
H.12.3	EW output voltage range		1.0	–	5.0	V
H.12.4	EW output current range		0	–	1200	μ A
EW PARABOLA/WIDTH						
H.13.1	control range	63 steps	0	–	22	%
H.13.2	equivalent output current	EW = 3FH	0	–	440	μ A
EW UPPER/LOWER CORNER/PARABOLA						
H.14.1	control range	63 steps	–43	–	0	%
H.14.2	equivalent output current	PW = 3FH; EW = 3FH	–190	–	0	μ A
EW TRAPEZIUM						
H.15.1	control range	63 steps	–5	–	+5	%
H.15.2	equivalent output current		–100	–	+100	μ A
VERTICAL AMPLITUDE						
H.16.1	control range	63 steps; SC = 00H	80	–	120	%
H.16.2	equivalent differential vertical drive output current (peak-to-peak value)	SC = 00H	760	–	1140	μ A
VERTICAL SHIFT						
H.17.1	control range	63 steps	–5	–	+5	%
H.17.2	equivalent differential vertical drive output current (peak-to-peak value)		–50	–	+50	μ A
S-CORRECTION						
H.18.1	control range	63 steps	0	–	30	%
VERTICAL ZOOM MODE (OUTPUT CURRENT VARIATION WITH RESPECT TO NOMINAL SCAN); NOTE 44						
H.19.1	vertical expand factor		0.75	–	1.38	
H.19.2	output current limiting and RGB blanking		–	1.05	–	

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Colour demodulation part						
CHROMINANCE AMPLIFIER						
D.1.1	ACC control range	note 45	26	–	–	dB
D.1.2	change in amplitude of the output signals over the ACC range		–	–	2	dB
D.1.3	threshold colour killer ON		–30	–	–	dB
D.1.4	hysteresis colour killer OFF	strong signal conditions; S/N ≥ 40 dB; note 6	–	+3	–	dB
D.1.5		noisy input signals; note 6	–	+1	–	dB
ACL CIRCUIT; NOTE 46						
D.2.1	chrominance burst ratio at which the ACL starts to operate		–	3.0	–	
REFERENCE PART						
Phase-locked loop						
D.3.1	catching range		±500	tbf	–	Hz
D.3.2	phase shift for a ±400 Hz deviation of the oscillator frequency	note 6	–	–	2	deg
HUE CONTROL						
D.5.1	hue control range	63 steps; see Fig.45	±35	±40	–	deg
D.5.2	hue variation for ±10% V _P	note 6	–	0	–	deg
D.5.3	hue variation with temperature	T _{amb} = 0 to 70 °C; note 6	–	0	–	deg
DEMODULATORS						
General						
D.6.3	spread of signal amplitude ratio between standards	note 6	–1	–	+1	dB
D.6.5	bandwidth of demodulators	–3 dB; note 47	–	650	–	kHz
PAL/NTSC demodulator						
D.6.6	gain between both demodulators G(B–Y) and G(R–Y)		1.60	1.78	1.96	
D.6.12	change of output signal amplitude with temperature	note 6	–	0.1	–	%/K
D.6.13	change of output signal amplitude with supply voltage	note 6	–	–	±0.1	dB
D.6.14	phase error in the demodulated signals	note 6	–	–	±5	deg

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SECAM demodulator						
D.7.1	black level off set		–	–	7	kHz
D.7.2	pole frequency of deemphasis		77	85	93	kHz
D.7.3	ratio pole and zero frequency		–	3	–	
D.7.4	non linearity		–	–	3	%
D.7.5	calibration voltage		1.7	2.3	2.7	V
Base-band delay line						
D.8.1	variation of output signal for adjacent time samples at constant input signals		–0.1	–	0.1	dB
D.8.2	residual clock signal (peak-to-peak value)		–	–	5	mV
D.8.3	delay of delayed signal		63.94	64.0	64.06	μs
D.8.4	delay of non-delayed signal		40	60	80	ns
D.8.5	difference in output amplitude with delay on or off		–	–	5	%
COLOUR DIFFERENCE MATRICES (IN CONTROL CIRCUIT)						
PAL/SECAM mode; (R–Y) and (B–Y) not affected						
D.9.1	ratio of demodulated signals (G–Y)/(R–Y)		–	–0.51 ±10%	–	
D.9.2	ratio of demodulated signals (G–Y)/(B–Y)		–	–0.19 ±25%	–	
NTSC mode; the matrix results in the following signals (nominal hue setting)						
MUS-bit = 0						
D.9.6	(B–Y) signal: 2.03/0°		2.03U _R			
D.9.7	(R–Y) signal: 1.59/95°		–0.14U _R + 1.58V _R			
D.9.8	(G–Y) signal: 0.61/240°		–0.31U _R – 0.53V _R			
MUS-bit = 1						
D.9.9	(B–Y) signal: 2.20/–1°		2.20U _R – 0.04V _R			
D.9.10	(R–Y) signal: 1.53/99°		–0.24U _R + 1.51V _R			
D.9.11	(G–Y) signal: 0.70/223°		–0.51U _R – 0.48V _R			
REFERENCE SIGNAL OUTPUT/SWITCH OUTPUT, PIN 32; NOTE 48						
D.10.1	reference frequency	CMB1/CMB0 = 01	3.58/4.43			MHz
D.10.2	output signal amplitude (peak-to-peak value)	CMB1/CMB0 = 01	0.2	0.25	0.3	V
D.10.3	output level (mid position)	CMB1/CMB0 = 01	tbf	4.0	tbf	V
D.10.4	output level LOW	CMB1/CMB0 = 10	–	–	0.8	V
D.10.5	output level HIGH	CMB1/CMB0 = 11	7.5	–	–	V

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Control part						
SATURATION CONTROL; NOTE 30						
C.1.1	saturation control range	63 steps; see Fig.46	52	–	–	dB
CONTRAST CONTROL; NOTE 30						
C.2.1	contrast control range	63 steps; see Fig.47	–	20	–	dB
C.2.2	tracking between the three channels over a control range of 10 dB		–	–	0.5	dB
C.2.6	contrast reduction		–	6	–	dB
BRIGHTNESS CONTROL						
C.3.1	brightness control range	63 steps; see Fig.48	–	± 0.7	–	V
RGB AMPLIFIERS						
C.4.1	output signal amplitude (peak-to-peak value)	at nominal luminance input signal, nominal contrast and white-point adjustment;	tbf	2.0	tbf	V
C.4.2	maximum signal amplitude (black-to-white)	note 49	–	tbf	–	V
C.4.3	input signal amplitude (CVBS/Y-input, pins 38 or 41) at which the soft clipping is activated	note 49	–	tbf	–	V
C.4.4	output signal amplitude for the 'red' channel (peak-to-peak value)	at nominal settings for contrast and saturation control and no luminance signal to the input (R–Y, PAL)	tbf	2.1	tbf	V
C.4.5	nominal black level voltage		–	2.5	–	V
C.4.6	black level voltage	when black level stabilisation is switched-off (via AKB bit)	–	2.5	–	V
C.4.61	black level voltage control range	VSD bit active; note 50	1.8	2.5	3.2	V
C.4.7	width of video blanking with HBL bit active	note 51	15.3	15.6	15.9	μ s
C.4.8	control range of the black-current stabilisation		–	± 1	–	V
C.4.9	blanking level	difference with black level, note 49	–	–0.5	–	V
C.4.10	level during leakage measurement		–	–0.1	–	V
C.4.11	level during 'low' measuring pulse		–	0.25	–	V
C.4.12	level during 'high' measuring pulse		–	0.38	–	V
C.4.13	adjustment range of the ratio between the amplitudes of the RGB drive voltage and the measuring pulses	note 49	–	± 3	–	dB

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB AMPLIFIERS (CONTINUED)						
C.4.14	variation of black level with temperature	note 6	–	1.0	–	mV/K
C.4.141	black level off set adjustment on the Red and Blue channel	15 steps	tbf	±40	tbf	mV
C.4.15	relative variation in black level between the three channels during variations of	note 6				
C.4.16	supply voltage (±10%)	nominal controls	–	–	tbf	mV
C.4.17	saturation (50 dB)	nominal contrast	–	–	tbf	mV
C.4.18	contrast (20 dB)	nominal saturation	–	–	tbf	mV
C.4.19	brightness (±0.5 V)	nominal controls	–	–	tbf	mV
C.4.20	temperature (range 40 °C)		–	–	tbf	mV
C.4.21	signal-to-noise ratio of the output signals	RGB input; note 52	60	–	–	dB
C.4.22		CVBS input; note 52	50	–	–	dB
C.4.23	residual voltage at the RGB outputs (peak-to-peak value)	at f _{osc}	–	–	15	mV
C.4.24		at 2f _{osc} plus higher harmonics	–	–	15	mV
C.4.25	bandwidth of output signals	RGB input; at –3 dB	tbf	15	–	MHz
C.4.26		CVBS input; at –3 dB; f _{osc} = 3.58 MHz	–	2.8	–	MHz
C.4.27		CVBS input; at –3 dB; f _{osc} = 4.43 MHz	–	3.4	–	MHz
C.4.28		S-VHS input; at –3 dB	5	–	–	MHz
WHITE-POINT ADJUSTMENT						
C.5.1	I ² C-bus setting for nominal gain	HEX code	–	20H	–	
C.5.2	adjustment range of RGB drive levels	note 53	–	±3	–	dB
C.5.3	gain control range to compensate spreads in picture tube characteristics		–	±6	–	dB
2-POINT BLACK-CURRENT STABILIZATION, NOTE 54						
C.6.1	amplitude of 'low' reference current		–	8	–	μA
C.6.2	amplitude of 'high' reference current		–	20	–	μA
C.6.3	acceptable leakage current		–	±100	–	μA
C.6.4	maximum current during scan		–	tbf	–	mA
C.6.5	input impedance		–	tbf	–	Ω

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NUMBER	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BEAM CURRENT LIMITING, NOTE 55						
C.7.1	contrast reduction starting voltage		–	3.5	–	V
C.7.2	voltage difference for full contrast reduction		–	2	–	V
C.7.3	brightness reduction starting voltage		–	2.5	–	V
C.7.4	voltage difference for full brightness reduction		–	1	–	V
C.7.5	internal bias voltage		–	3.3	–	V
C.7.6	detection level vertical guard		–	3.65	–	V
C.7.7	minimum input current to activate the guard circuit		–	tbf	–	mA
C.7.8	maximum allowable current		–	tbf	–	mA
FIXED BEAM CURRENT SWITCH-OFF; NOTE 56						
C.8.1	discharge current during switch-off		0.85	1.0	1.15	mA
C.8.2	discharge time of picture tube		–	38	–	ms

Notes

- When the 3.3 V supply is present and the μ -Controller is active a 'low-power start-up' mode can be activated. When all sub-address bytes have been sent and the POR and XPR flags have been cleared the horizontal output can be switched-on via the STB-bit (subaddress 24H). In this condition the horizontal drive signal has the nominal T_{OFF} and the T_{ON} grows gradually from zero to the nominal value. As soon as the 8 V supply is present the switch-on procedure (e.g. closing of the second loop) is continued.
- On set AGC.
- This parameter is not tested during production and is just given as application information for the designer of the television receiver.
- Loop bandwidth $BL = 60$ kHz (natural frequency $f_N = 15$ kHz; damping factor $d = 2$; calculated with top sync level as FPLL input signal level).
- The IF-PLL demodulator uses an internal VCO (no external LC-circuit required) which is calibrated by means of a digital control circuit which uses the clock frequency of the μ -Controller as a reference. The required IF frequency for the various standards is set via the IFA-IFC bits in subaddress 27H. When the system is locked the resulting IF frequency is very accurate with a deviation from the nominal value of less than 25 kHz.
- This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.
- Measured at 10 mV (RMS) top sync input signal.
- Via this pin (38) both the demodulated IF signal and the selected CVBS (or Y+C) signal can be supplied to the output. The selection between both signals is realised by means of the SVO bit in subaddress 22H.
- So called projected zero point, i.e. with switched demodulator.
- Measured in accordance with the test line given in Fig.49. For the differential phase test the peak white setting is reduced to 87%.

The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.

The phase difference is defined as the difference in degrees between the largest and smallest phase angle.

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11. This figure is valid for the complete video signal amplitude (peak white-to-black), see Fig.50.
12. The noise inverter is only active in the 'strong signal mode' (no noise detected in the incoming signal)
13. Measured at an input signal of 10 mV_{RMS}. The S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value). B = 5 MHz. Weighted in accordance with CCIR 567.
14. The time-constant of the IF-AGC is internal and the speed of the AGC can be set via the bits AGC1 and AGC0 in subaddress 28H. The AGC response time is also dependent on the acquisition time of the PLL demodulator. The values given are valid for the 'norm' setting (AGC1-AGC0 = 0-1) and when the PLL is in lock.
15. The AFC control voltage is generated by the digital tuning system of the PLL demodulator. This system uses the clock frequency of the μ -Controller/Teletext decoder as a reference and is therefore very accurate. For this reason no maximum and minimum values are given for the window sensitivity figures (parameters M.7.2 and M.7.3). The tuning information is supplied to the tuning system via the AFA and AFB bits in output byte 02H. The AFC value is valid only when the LOCK-bit is 1.
16. The weighted S/N ratio is measured under the following conditions:
 - a) The vision IF modulator must meet the following specifications:
 Incidental phase modulation for black-to-white jumps less than 0.5 degrees.
 QSS AF performance, measured with the television-demodulator AMF2 (audio output, weighted S/N ratio) better than 60 dB (deviation 27 kHz) for 6 kHz sine wave black-to-white modulation.
 Picture-to-sound carrier ratio: PC/SC1 = 13 dB (transmitter).
 - b) The measurements must be carried out with the Siemens SAW filters G3962 for vision IF and G9350 for sound IF. Input level for sound IF 10 mV_{RMS} with 27 kHz deviation.
 - c) The PC/SC ratio at the vision IF input is calculated as the addition of the TV transmitter ratio and the SAW filter PC/SC ratio. This PC/SC ratio is necessary to achieve the S/N(W) values as indicated.
17. Calculation of the FM-PLL filter can be done approximately by use of the following equations:

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{K_0 K_D}{C_P}}$$

$$\nu = \frac{1}{2R \sqrt{K_0 K_D C_P}}$$

$$BL_{-3dB} = f_0(1.55 - \nu^2)$$

These equations are only valid under the conditions that $\nu \leq 1$ and $C_S > 5C_P$.

Definitions:

K_0 = VCO steepness in rad/V

K_D = phase detector steepness μ A/rad

R = loop filter resistor

C_S = series capacitor

C_P = parallel capacitor

f_0 = natural frequency of PLL

BL_{-3dB} = loop bandwidth for -3dB

ν = damping factor

Some examples for these values are given in table 121

18. Modulation frequency: 1 kHz, $\Delta f = \pm 50$ kHz.
19. $f = 4.5/5.5$ MHz; FM: 70 Hz, ± 50 kHz deviation; AM: 1.0 kHz, 30% modulation.

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20. This figure is independent of the TV standard and valid for a frequency deviation of ± 25 kHz at a carrier frequency of 4.5 MHz or a deviation of ± 50 kHz at a carrier frequency of 5.5/6.0/6.5 MHz.
21. The deemphasis pin can also be used as additional audio input. In that case the internal (demodulated FM signal) must be switched off. This can be realised by means of the SM (sound mute) bit. When the vision IF amplifier is switched to positive modulation the signal from the FM demodulator is automatically switched off. The external signal on pin 28 must be switched off when the internal signal is selected.
22. $f = 5.5$ MHz; FM: 1 kHz, ± 17.5 kHz deviation. Measured with a bandwidth of 15 kHz and the audio attenuator at -6 dB.
23. $f = 4.5$ MHz, FM: 1 kHz, ± 100 kHz deviation and the volume control setting such that no clipping occurs in the audio output.
24. Unweighted RMS value, $V_i = 100$ mV_{RMS}, FM: 1 kHz, ± 50 kHz deviation, audio attenuator at -6 dB.
25. Audio attenuator at -20 dB; temperature range 10 to 50 °C.
26. In various versions the Automatic Volume Levelling (AVL) function can be activated. The pin to which the external capacitor has to be connected depends on the IC version. For the 90° types the capacitor is connected to the EW output pin (pin 20). For the 110° types a choice can be made between the AVL function and a sub-carrier output / general purpose switch output. The selection must be made by means of the CMB0 and CMB1 bit in subaddress 22H (see also table G-1 on page G-9). More details about the sub-carrier output are given in the parameters D.10.
The Automatic Volume Levelling (AVL) circuit stabilises automatically the audio output signal to a certain level which can be set by means of the volume control. This AVL function prevents big audio output fluctuations due to variation of the modulation depth of the transmitter. The AVL can be switched on and off via the AVL bit in subaddress 29H.
The AVL is active over an input voltage range (measured at the deemphasis output) of 150 to 1500 mV_{RMS}. The AVL control curve is given in Fig.51. The control range of $+6$ dB to -14 dB is valid for input signals with 50% of the maximum frequency deviation.
27. Signal with negative-going sync. Amplitude includes sync pulse amplitude.
28. This parameter is measured at nominal settings of the various controls.
29. Indicated is a signal for a colour bar with 75% saturation (chroma : burst ratio = 2.2 : 1).
30. The contrast and saturation control is active on the internal signal (YUV) and on the external RGB/YUV input. The Text/OSD input can be controlled on brightness only. Nominal contrast is specified with the DAC in position 20 HEX. Nominal saturation as maximum -10 dB.
31. The YUV input signal amplitudes are based on a colour bar signal with 75% saturation.
32. When the decoder is forced to a fixed subcarrier frequency (via the CM-bits) the chroma trap is always switched-on, also when no colour signal is identified. In the automatic mode the chroma trap is switched-off when no colour signal is identified.
33. Valid for a signal amplitude on the Y-input of 0.7 V black-to-white (100 IRE) with a rise time (10% to 90%) of 70 ns and the video switch in the Y/C mode. During production the peaking function is not tested by measuring the overshoots but by measuring the frequency response of the Y output.
34. For video signals with a black level which deviates from the back-porch blanking level the signal is "stretched" to the blanking level. The amount of correction depends on the IRE value of the signal (see Fig.52). The black level is detected by means of an internal capacitor. The black level stretcher can be switched on and off via the BKS bit in subaddress 2DH. The values given in the specification are valid only when the luminance input signal has an amplitude of 1 V_{p-p}.
35. The slicing level is independent of sync pulse amplitude. The given percentage is the distance between the slicing level and the black level (back porch). When the amplitude of the sync pulse exceeds the value of 350 mV the sync separator will slice the sync pulse at a level of 175 mV above top sync. The maximum sync pulse amplitude is 4 V_{p-p}.

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36. To obtain a good performance for both weak signal and VCR playback the time constant of the first control loop is switched depending on the input signal condition and the condition of the POC, FOA, FOB and VID bits in subaddress 24H. The circuit contains a noise detector and the time constant is switched to 'slow' when too much noise is present in the signal. In the 'fast' mode during the vertical retrace time the phase detector current is increased 50% so that phase errors due to head-switching of the VCR are corrected as soon as possible. Switching of the time constant can be automatically or can be set by means of the control bits.

The circuit contains a video identification circuit which is independent of the first loop. This identification circuit can be used to close or open the first control loop when a video signal is present or not present on the input. This enables a stable On Screen Display (OSD) when just noise is present at the input.

To prevent that the horizontal synchronisation is disturbed by anti copy signals like Macrovision the phase detector is gated during the vertical retrace period so that pulses during scan have no effect on the output voltage. The width of the gate pulse is about 22 μ s. During weak signal conditions (noise detector active) the gating is active during the complete scan period and the width of the gate pulse is reduced to 5.7 μ s so that the effect of noise is reduced to a minimum.

The output current of the phase detector in the various conditions are shown in Table 122.

37. The ICs have 2 protection inputs. The protection on the second phase detector pin is intended to be used as 'flash' protection. When this protection is activated the horizontal drive is switched-off immediately and then switched-on again via the slow start procedure.

The protection on the EHT input is intended for overvoltage (X-ray) protection. When this protection is activated the horizontal drive is directly switched-off (via the slow stop procedure).

The EHT protection input can also be used to switch-off the TV receiver in a correct way when it is switched off via the mains power switch or when the power supply is interrupted by pulling the mains plug. This can be realised by means of a detection circuit which monitors the main supply voltage of the receiver. When this voltage suddenly decreases the EHT protection input must be pulled HIGH and then the horizontal drive is switched off via the slow stop procedure. Whether the EHT capacitor is discharged in the overscan or not during the switch-off period depends on the setting of the OSO bit (subaddress 25H, D4). See also note 56.

38. The control range indicates the maximum phase difference at the top and the bottom of the screen. Compared with the phase position at the centre of the screen the maximum phase difference at the top and the bottom of the screen is $\pm 0.5 \mu$ s.

39. During switch-on the horizontal drive starts-up in a soft-start mode. The horizontal drive starts with a very short T_{ON} time of the horizontal output transistor, the 'off time' of the transistor is identical to the 'off time' in normal operation. The starting frequency during switch-on is therefore about 2 times higher than the normal value. The 'on time' is slowly increased to the nominal value. When the nominal frequency is reached the PLL is closed in such a way that only very small phase corrections are necessary. This ensures a safe operation of the output stage. The switch-on characteristic is given in Fig.54

During switch-off the soft-stop function is active. This is realised by decreasing the T_{ON} of the output transistor complimentary to the start-up behaviour. The switch-off time is about 43 ms. The soft-stop procedure is synchronised to the start of the first new vertical field after the reception of the switch-off command. Furthermore the EHT capacitor of the picture tube is discharged with a fixed beam current which is forced by the black current loop. The discharge time is about 38 ms. During switch-off the vertical scan is stopped so that the discharge takes place in the overscan.

The horizontal output is gated with the flyback pulse so that the horizontal output transistor cannot be switched-on during the flyback time.

40. The vertical blanking pulse in the RGB outputs has a width of 26 or 21 lines (50 or 60 Hz system). The vertical pulse in the sandcastle pulse has a width of 14 lines. This to prevent a phase distortion on top of the picture due to a timing modulation of the incoming flyback pulse.

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41. The timing pulses for the vertical ramp generator are obtained from the horizontal oscillator via a divider circuit. During TV reception this divider circuit has 3 modes of operation:
 - a) Search mode 'large window'.

This mode is switched on when the circuit is not synchronized or when a non-standard signal (number of lines per frame outside the range between 311 and 314(50 Hz mode) or between 261 and 264 (60 Hz mode) is received). In the search mode the divider can be triggered between line 244 and line 361 (approximately 45 to 64.5 Hz).
 - b) Standard mode 'narrow window'.

This mode is switched on when more than 15 succeeding vertical sync pulses are detected in the narrow window. When the circuit is in the standard mode and a vertical sync pulse is missing the retrace of the vertical ramp generator is started at the end of the window. Consequently, the disturbance of the picture is very small. The circuit will switch back to the search window when, for 6 successive vertical periods, no sync pulses are found within the window.
 - c) Standard TV-norm (divider ratio 525 (60 Hz) or 625 (50 Hz)).

When the system is switched to the narrow window it is checked whether the incoming vertical sync pulses are in accordance with the TV-norm. When 15 standard TV-norm pulses are counted the divider system is switched to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing.

When 3 vertical sync pulses are missed the system switches back to the narrow window and when also in this window no sync pulses are found (condition 3 missing pulses) the system switches over to the search window.

The vertical divider needs some waiting time during channel-switching of the tuner. When a fast reaction of the divider is required during channel-switching the system can be forced to the search window by means of the NCIN bit in subaddress 25H.

When RGB signals are inserted the maximum vertical frequency is increased to 72 Hz. This has the consequence that the circuit can also be synchronised by signals with a higher vertical frequency like VGA.
42. Conditions: frequency is 50 Hz; normal mode; VS = 1F.
43. The output range percentages mentioned for E-W control parameters are based on the assumption that 400 μ A variation in E-W output current is equivalent to 20% variation in picture width.
44. The ICs have a zoom adjustment possibility for the horizontal and vertical deflection. For this reason an extra DAC has been added in the vertical amplitude control which controls the vertical scan amplitude between 0.75 and 1.38 of the nominal scan. At an amplitude of 1.06 of the nominal scan the output current is limited and the blanking of the RGB outputs is activated. This is illustrated in Fig.53.

The nominal scan height must be adjusted at a position of 19 HEX of the vertical 'zoom' DAC.
45. At a chrominance input voltage of 660 mV (p-p) (colour bar with 75% saturation i.e. burst signal amplitude 300 mV (p-p)) the dynamic range of the ACC is +6 and -20 dB.
46. The ACL function can be activated by via the ACL bit in the subaddress 20H. The ACL circuit reduces the gain of the chroma amplifier for input signals with a chroma-to-burst ratio which exceeds a value of 3.0.
47. This parameter indicates the bandwidth of the complete chrominance circuit including the chrominance bandpass filter. The bandwidth of the low-pass filter of the demodulator is approximately 1 MHz.
48. The subcarrier output is combined with a 3-level switch output which can be used to switch external circuits like sound traps etc. This output is controlled by the CMB1 and CMB0 bits in control byte 22H. The subcarrier signal is available when CMB1/0 are set to 0/1. When CMB1/0 are set to 00 in versions for 90° picture tubes (no EW output) this pin is switched to external sound IF input.
49. Because of the 2-point black current stabilization circuit both the black level and the amplitude of the RGB output signals depend on the drive characteristic of the picture tube. The system checks whether the returning measuring currents meet the requirement and adapts the output level and gain of the circuit when necessary. Therefore the typical value of the black level and amplitude at the output are just given as an indication for the design of the RGB output stage.

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The 2-point black level system adapts the drive voltage for each cathode in such a way that the 2 measuring currents have the right value. This has the consequence that a change in the gain of the output stage will be compensated by a gain change of the RGB control circuit. Because different picture tubes may require different drive voltage amplitudes the ratio between the output signal amplitude and the inserted measuring pulses can be adapted via the I²C-bus. This is indicated in the parameter Adjustment range of the ratio between the amplitudes of the RGB drive voltage and the measuring pulses'.

Because of the dependence of the output signal amplitude on the application the soft clipping limiting has been related to the input signal amplitude.

50. For the alignment of the picture tube the vertical scan can be stopped by means of the VSD bit. In that condition a certain black level is inserted at the RGB outputs. The value of this level can be adjusted by means of the brightness control DAC. An automatic adjustment of the V_{g2} of the picture tube can be realised by using the WBC and HBC bits in output byte 01. For a black level feedback current between 2 and 5 μ A the WBC = 1, for a higher or lower current WBC = 0. Whether the current is too high or too low can be found from the HBC bit.
51. When the reproduction of 4 : 3 pictures on a 16 : 9 picture tube is realised by means of a reduction of the horizontal scan amplitude the edges of the picture may slightly be disturbed. This effect can be prevented by adding an additional blanking to the RGB signals. The blanking pulse is derived from the horizontal oscillator and is directly related to the incoming video signal (independent of the flyback pulse). The additional blanking overlaps the normal blanking signal with about 1 μ s on both sides. This blanking is activated with the HBL bit.
52. Signal-to-noise ratio (S/N) is specified as peak-to-peak signal with respect to RMS noise (bandwidth 5 MHz).
53. When the black-current stabilization loop is switched off (AKB = 1) the WPA control range is reduced to ± 1 dB.
54. This is a current input. The start-up procedure is as follows.

When the TV receiver is switched-on the RGB outputs are blanked and the black-current loop will try to adjust the picture tube to the right bias levels. The RGB drive signals are switched-on as soon as the black current loop is stabilised. This results in the shortest switch-on time.

When this switch-on system results in a visible disturbance of the picture it is possible to add a further switch-on delay via a software routine. In that case the RGB outputs must be blanked by means of the RBL bit. As soon as the black current loop is stabilised the BCF-bit is set to 0 (output byte 01). This information can then be used to switch-on the RGB outputs with some additional delay.

55. The beam current limiting and the vertical guard function have been combined on this pin. The beam current limiting function is active during the vertical scan period.
56. During switch-off the magnitude of the discharge current of the picture tube is controlled by the black current loop. Dependent on the setting of the OSO bit the vertical scan can be stopped in an overscan position during that time so that the discharge is not visible on the screen. The switch-off procedure is as follows:
 - a) The vertical scan and retrace are completed
 - b) The soft-stop procedure is started with a reduction of the T_{ON} of the output stage from nominal to zero
 - c) The fixed beam current is forced via the black current loop
 - d) If OSO = 1 the vertical deflection stays in the overscan position
 - e) If OSO = 0 the vertical deflection will keep running during the switch-off time

Table 121 Some examples for the FM-PLL filter

BL _{-3dB} (kHz)	C _S (nF)	C _P (pF)	R (k Ω)	v
100	4.7	820	2.7	0.5
160	4.7	330	3.9	0.5

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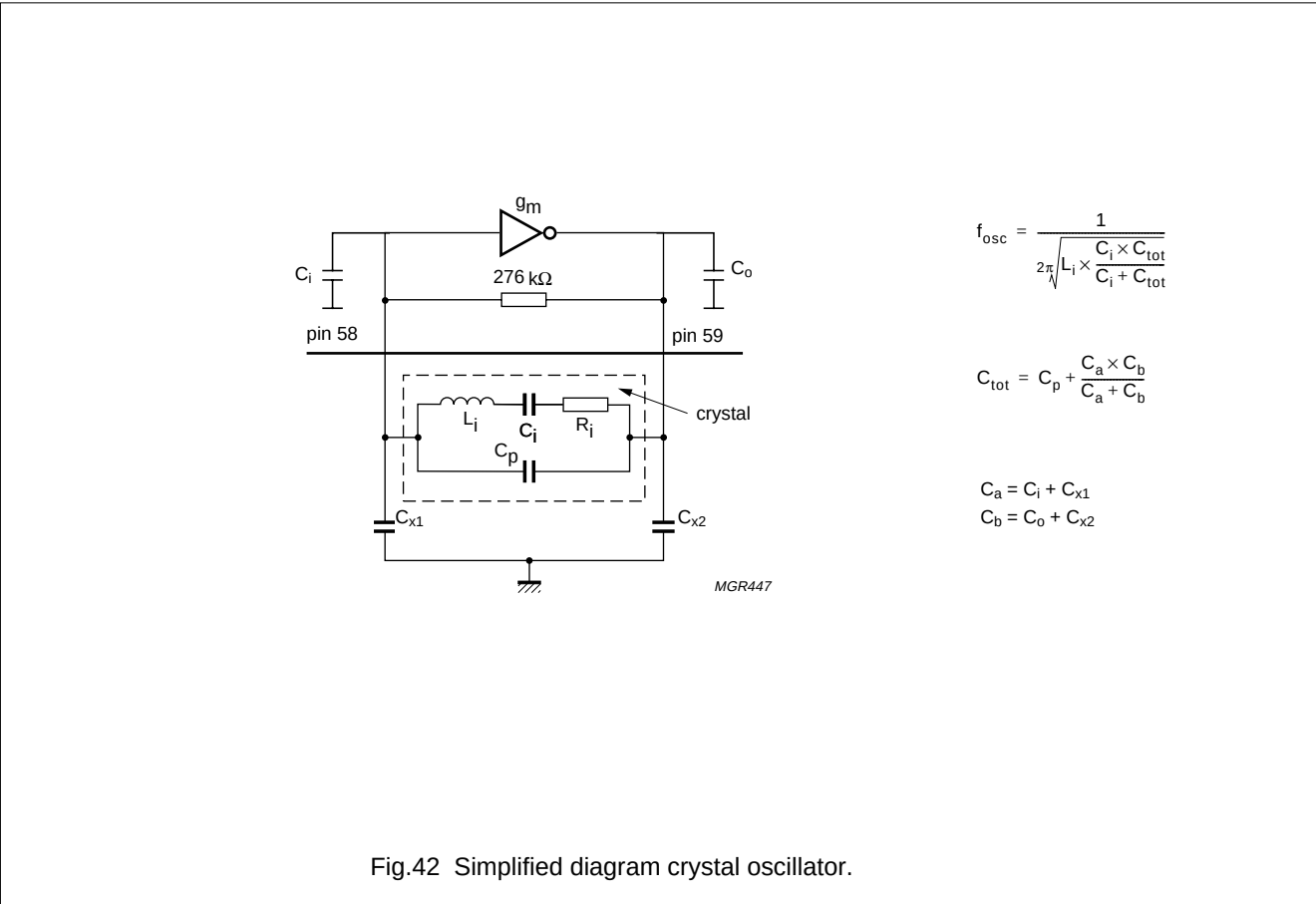
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Table 122 Output current of the phase detector in the various conditions

I ² C-BUS COMMANDS				IC CONDITIONS			ϕ -1 CURRENT/MODE			
VID	POC	FOA	FOB	IFI	SL	NOISE	SCAN	V-RETR	GATING	MODE
–	0	0	0	yes	yes	no	180	270	yes ⁽¹⁾	auto
–	0	0	0	yes	yes	yes	30	30	yes	auto
–	0	0	0	yes	no	–	180	270	no	auto
–	0	0	1	yes	yes	–	30	30	yes	slow
–	0	0	1	yes	no	–	180	270	no	slow
–	0	1	0	yes	yes	no	180	270	yes	fast
–	0	1	0	yes	yes	yes	30	30	yes	slow
–	–	1	1	–	–	–	180	270	no	fast
0	0	–	–	no	–	–	6	6	no	OSD
–	1	–	–	–	–	–	–	–	–	off

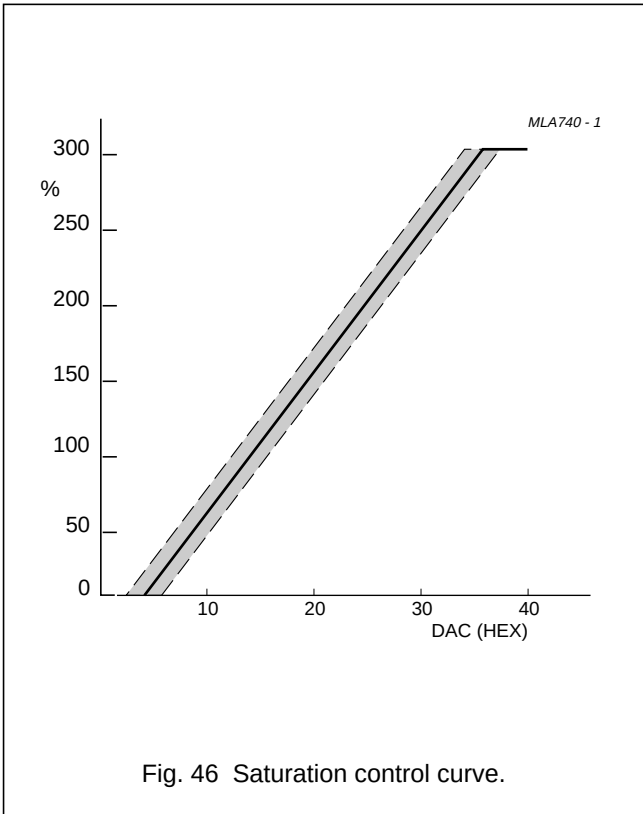
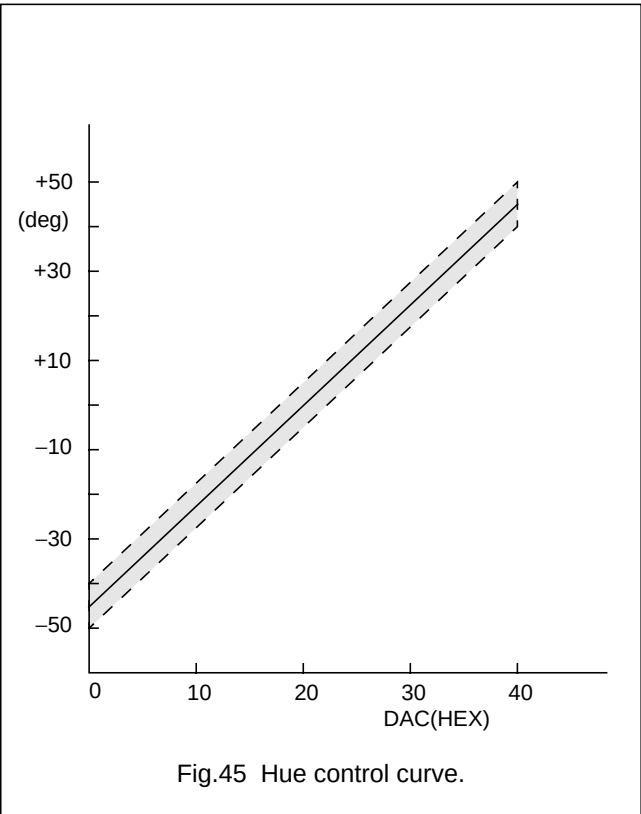
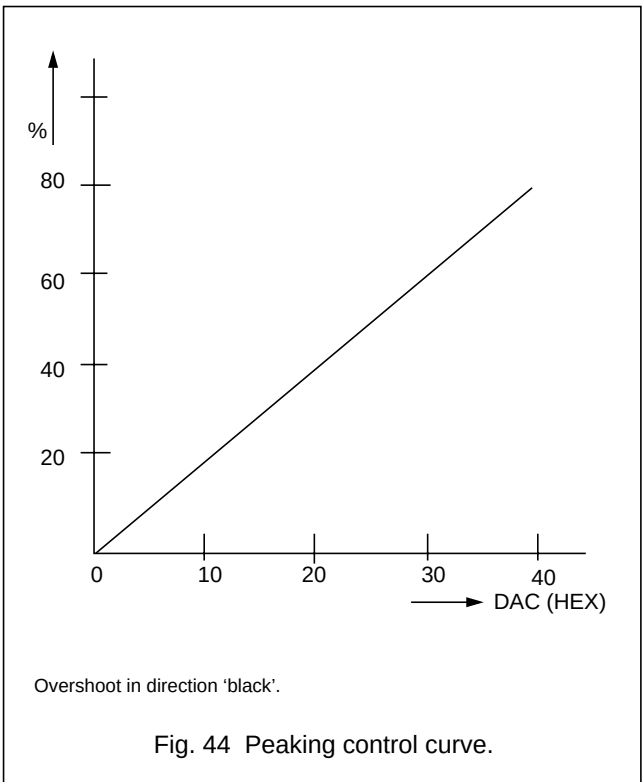
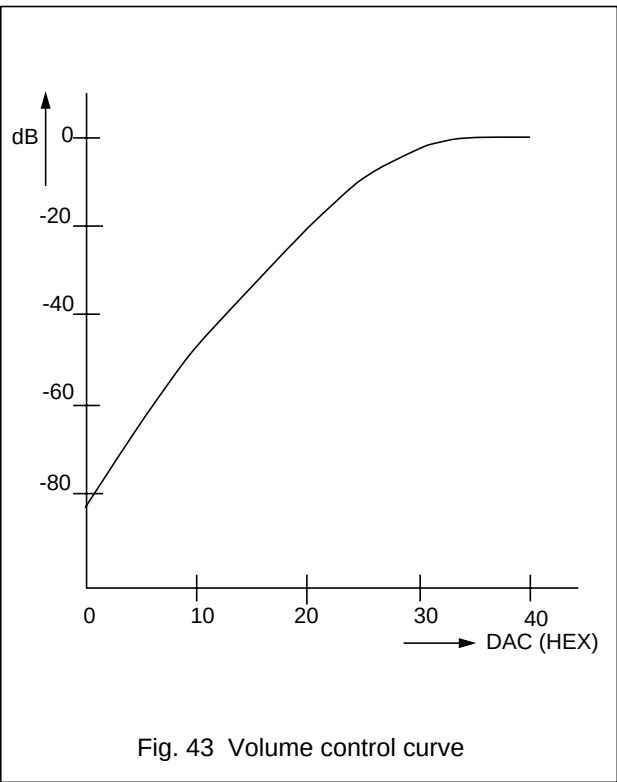
Note

1. Only during vertical retrace, width 22 μ s. In the other conditions the width is 5.7 μ s and the gating is continuous.



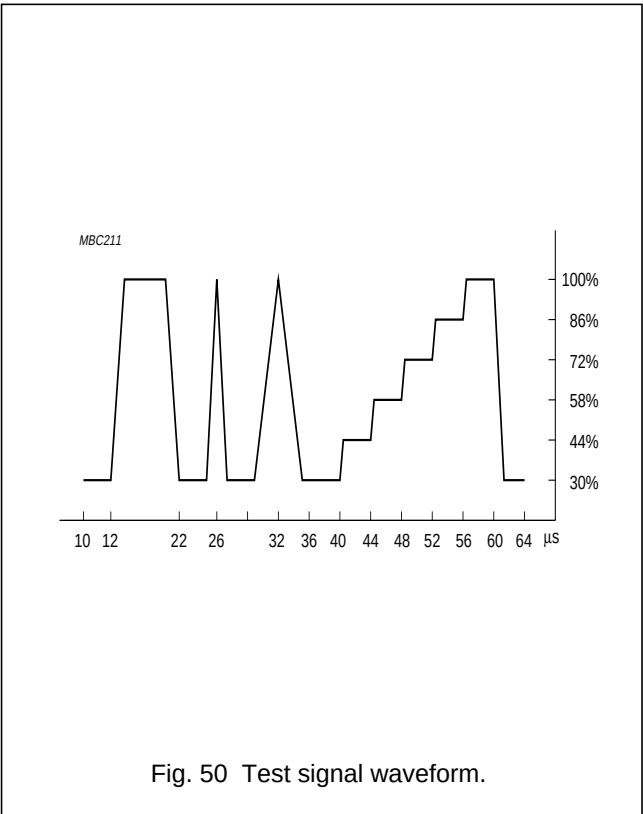
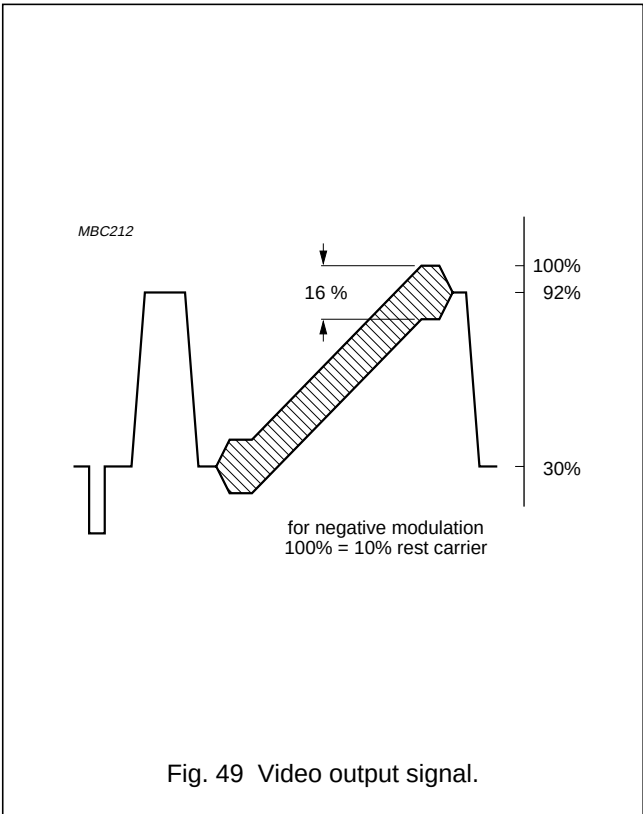
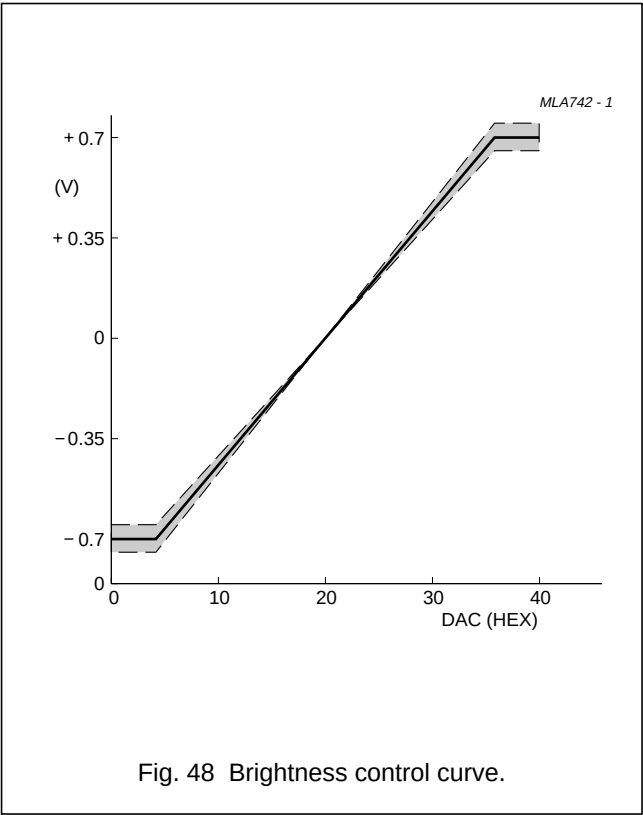
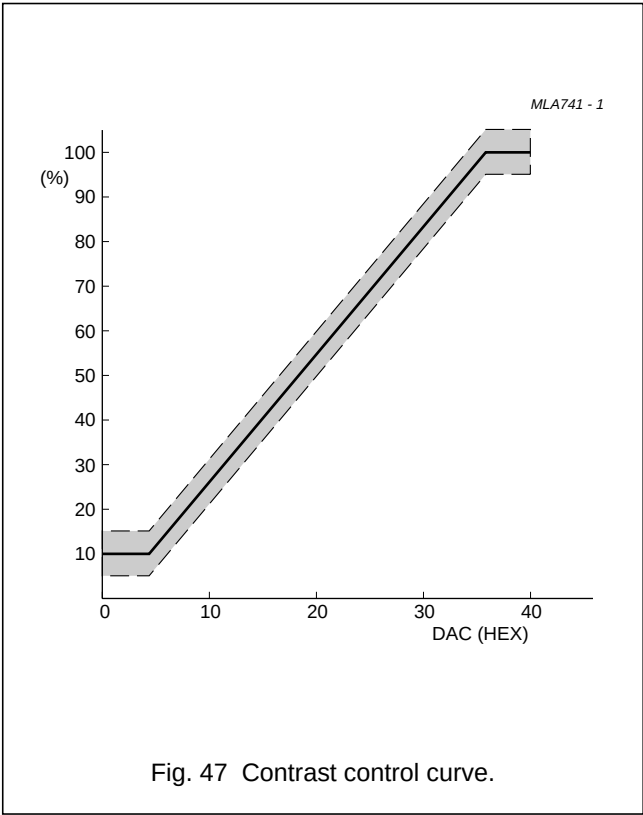
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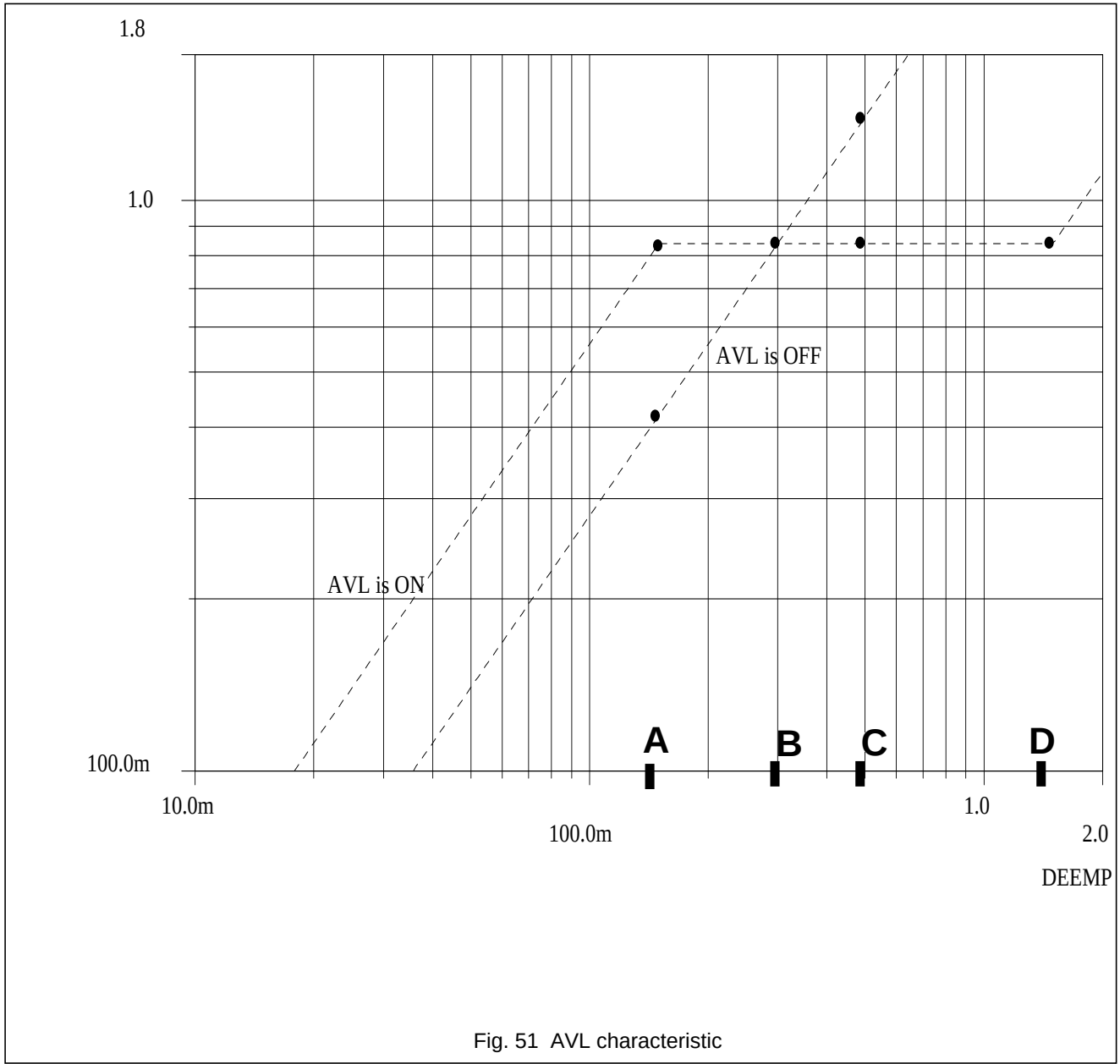
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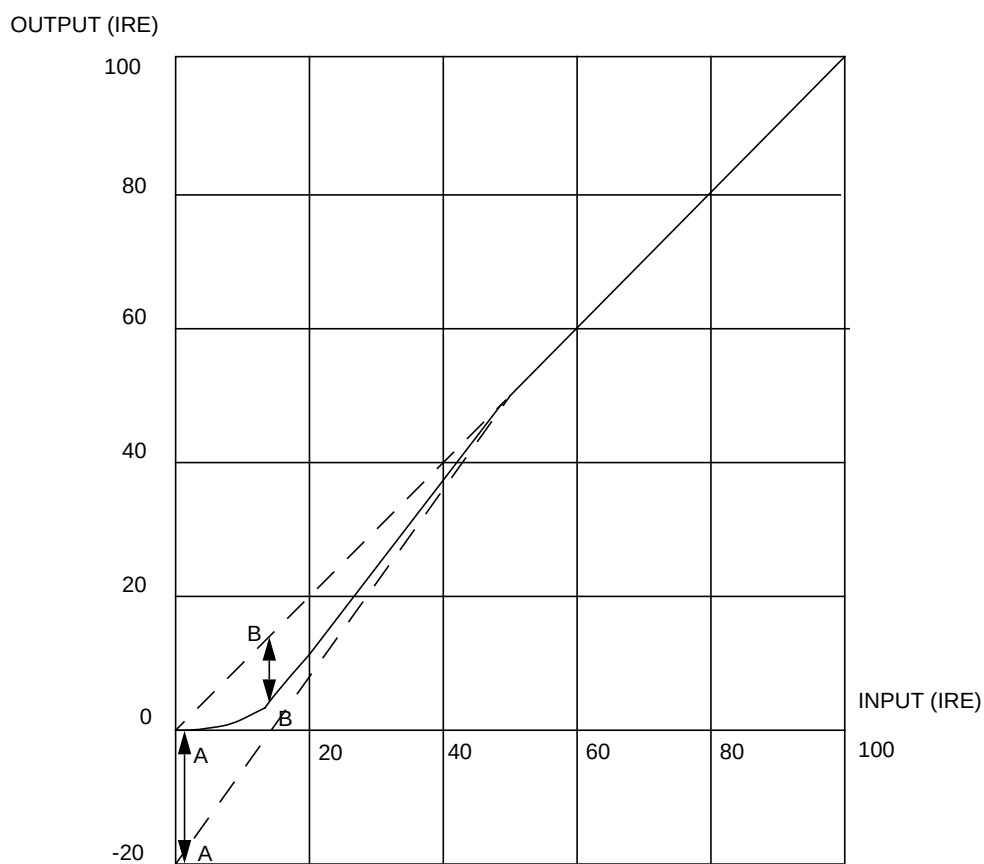
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CHARACTERISTIC POINTS AVL	A	B	C	D	UNIT
Deemphasis voltage	150	300	500	1500	mV _{RMS}
FM swing	15	30	50	150	kHz



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A-A: MAXIMUM BLACK LEVEL SHIFT

B-B: LEVEL SHIFT AT 15% OF PEAK WHITE

Fig. 52 I/O relation of the black level stretch circuit

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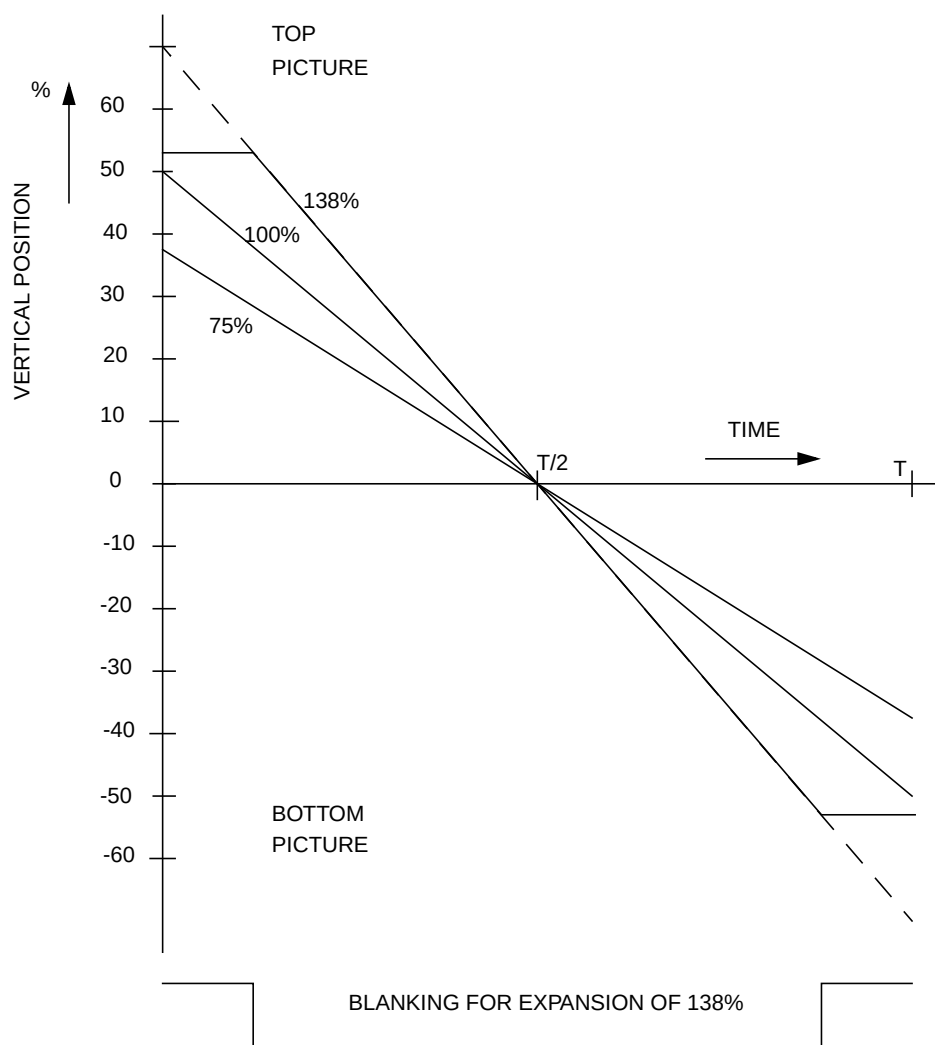
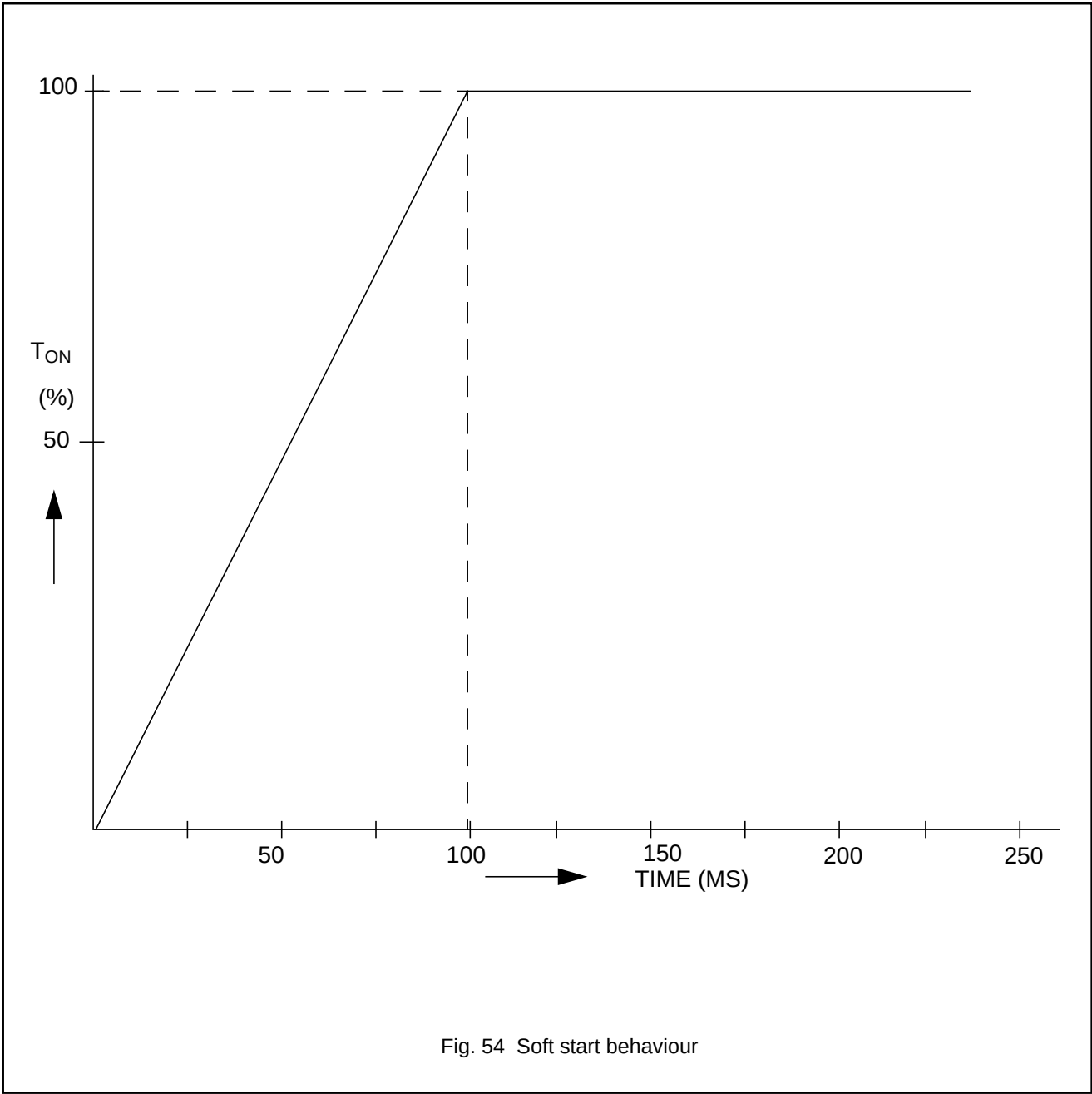


Fig. 53 Sawtooth waveform and blanking pulse for 110° types

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TEST AND APPLICATION INFORMATION

East-West output stage

In order to obtain correct tracking of the vertical and horizontal EHT-correction, the EW output stage should be dimensioned as illustrated in Fig.55.

Resistor R_{EW} determines the gain of the EW output stage. Resistor R_C determines the reference current for both the vertical sawtooth generator and the geometry processor. The preferred value of R_C is 39 k Ω which results in a reference current of 100 μ A ($V_{ref} = 3.9$ V).

The value of R_{EW} must be:

$$R_{EW} = R_C \times \frac{V_{scan}}{18 \times V_{ref}}$$

Example: With $V_{ref} = 3.9$ V; $R_C = 39$ k Ω and $V_{scan} = 120$ V then $R_{EW} = 68$ k Ω .

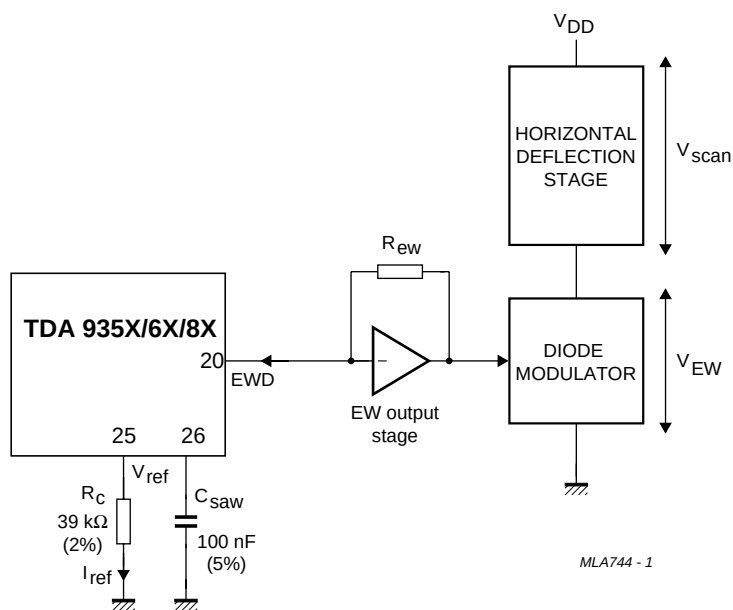
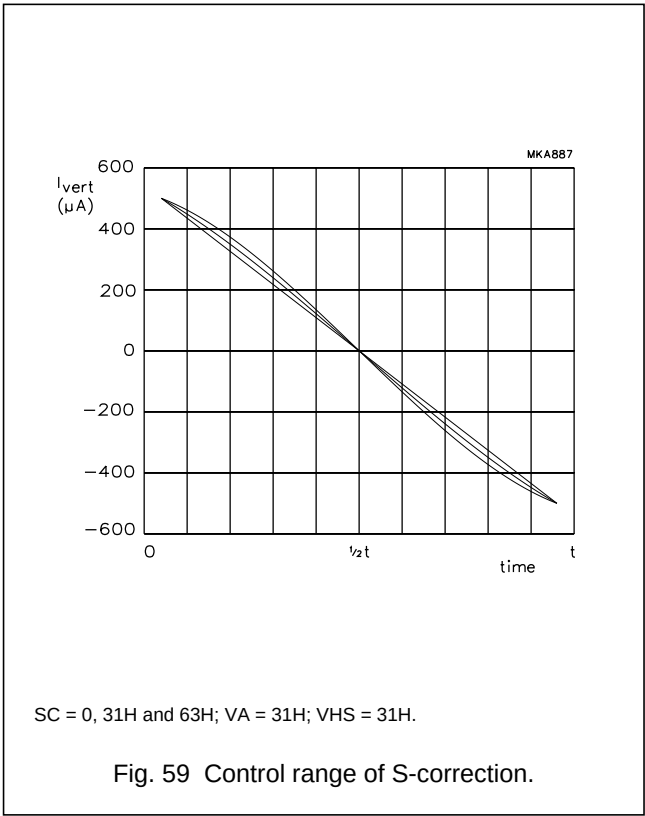
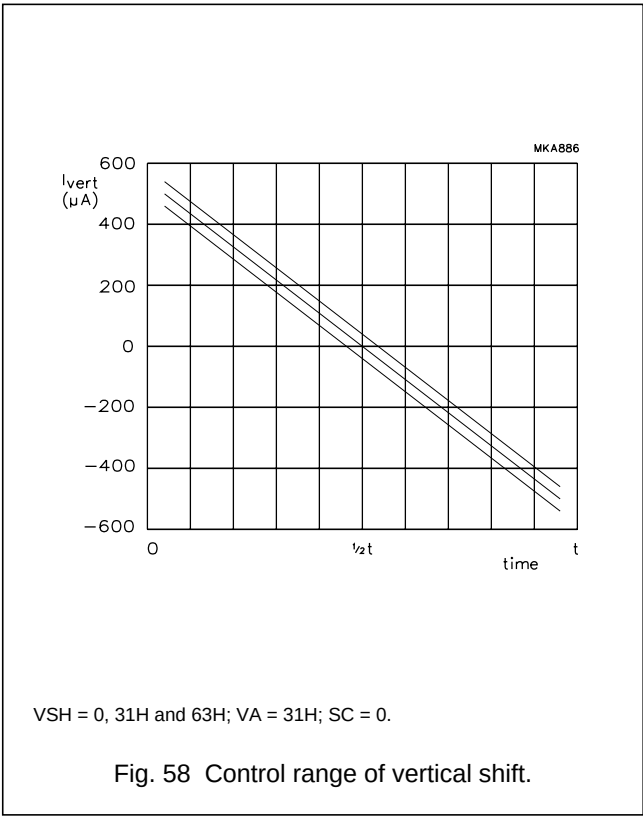
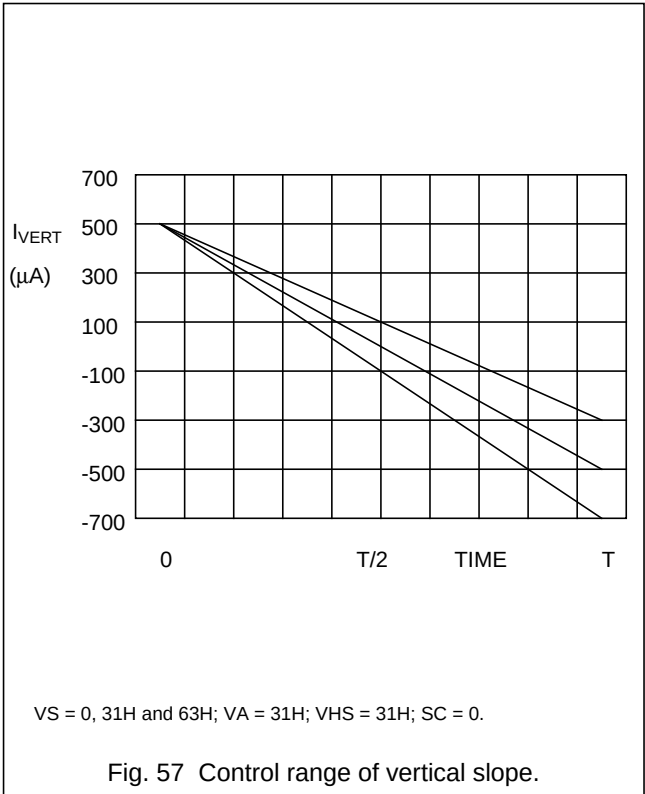
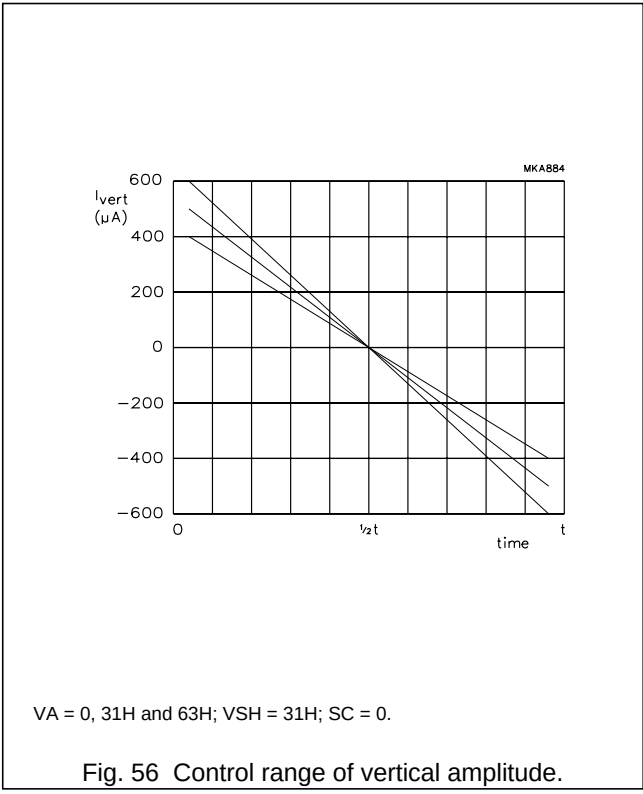


Fig. 55 East-West output stage.

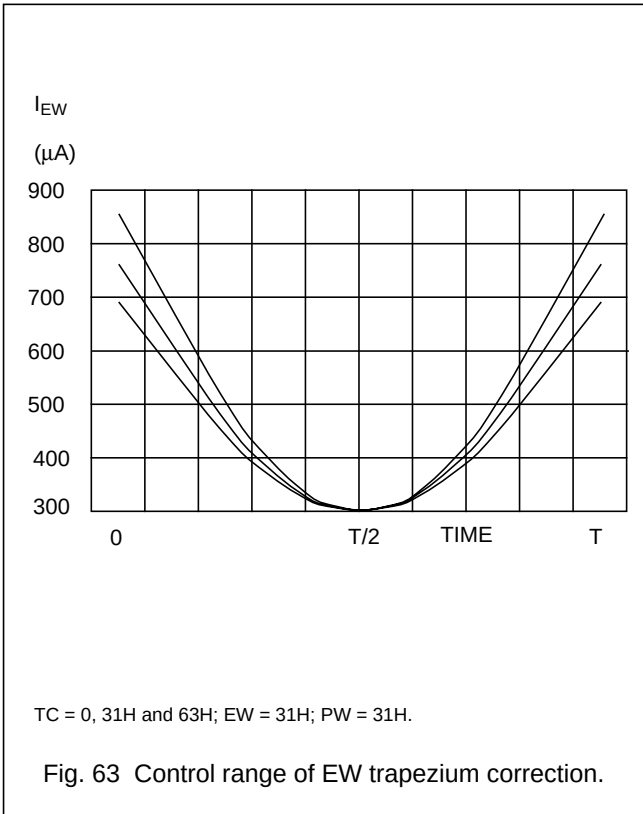
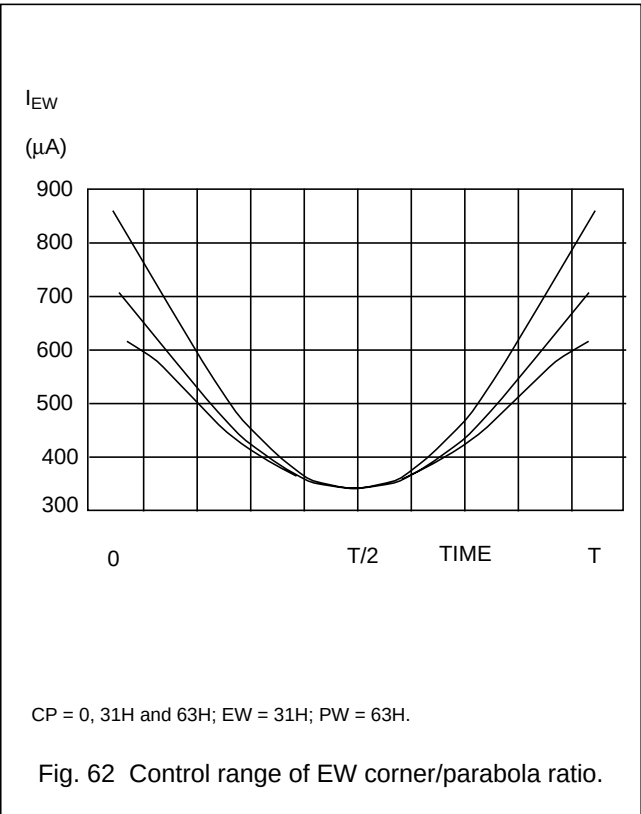
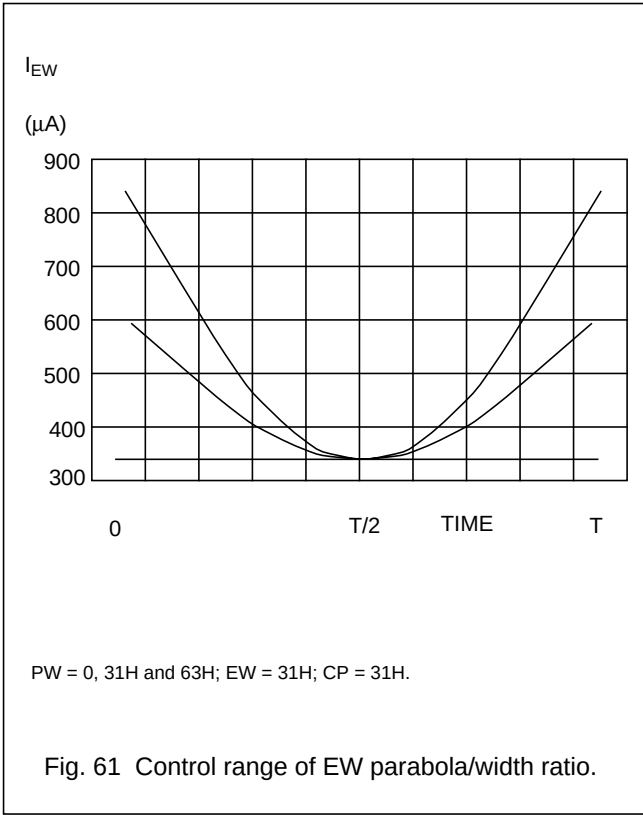
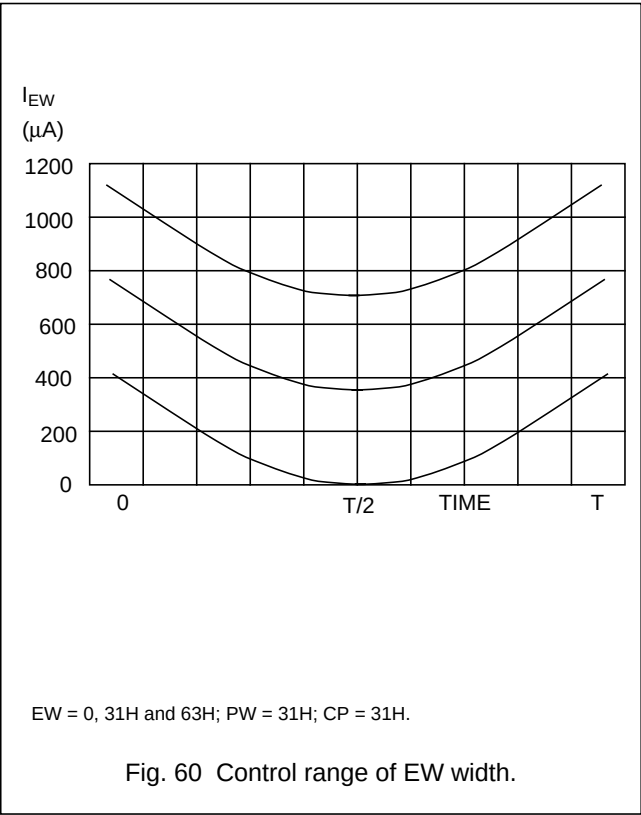
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Adjustment of geometry control parameters

The deflection processor offers 5 control parameters for picture alignment, viz:

- S-correction
- vertical amplitude
- vertical slope
- vertical shift
- horizontal shift.

The 110° types offer in addition:

- EW width
- EW parabola width
- EW upper/lower corner parabola
- EW trapezium correction.
- Vertical zoom
- Horizontal parallelogram and bow correction for some versions in the range

It is important to notice that the ICs are designed for use with a DC-coupled vertical deflection stage. This is the reason why a vertical linearity alignment is not necessary (and therefore not available).

For a particular combination of picture tube type, vertical output stage and EW output stage it is determined which are the required values for the settings of S-correction, EW parabola/width ratio and EW corner/parabola ratio. These parameters can be preset via the I²C-bus, and do not need any additional adjustment. The rest of the parameters are preset with the mid-value of their control range (i.e. 1FH), or with the values obtained by previous TV-set adjustments.

The vertical shift control is meant for compensation of off sets in the external vertical output stage or in the picture tube. It can be shown that without compensation these off sets will result in a certain linearity error, especially with picture tubes that need large S-correction. The total linearity error is in first order approximation proportional to the value of the off set, and to the square of the S-correction needed. The necessity to use the vertical shift alignment depends on the expected off sets in vertical output stage and picture tube, on the required value of the S-correction, and on the demands upon vertical linearity.

For adjustment of the vertical shift and vertical slope independent of each other, a special service blanking mode can be entered by setting the SBL bit HIGH. In this mode the RGB-outputs are blanked during the second half of the picture. There are 2 different methods for alignment of the picture in vertical direction. Both methods make use of the service blanking mode.

The first method is recommended for picture tubes that have a marking for the middle of the screen. With the vertical shift control the last line of the visible picture is positioned exactly in the middle of the screen. After this adjustment the vertical shift should not be changed. The top of the picture is placed by adjustment of the vertical amplitude, and the bottom by adjustment of the vertical slope.

The second method is recommended for picture tubes that have no marking for the middle of the screen. For this method a video signal is required in which the middle of the picture is indicated (e.g. the white line in the circle test pattern). With the vertical slope control the beginning of the blanking is positioned exactly on the middle of the picture. Then the top and bottom of the picture are placed symmetrical with respect to the middle of the screen by adjustment of the vertical amplitude and vertical shift. After this adjustment the vertical shift has the right setting and should not be changed.

If the vertical shift alignment is not required VSH should be set to its mid-value (i.e. VSH = 1F). Then the top of the picture is placed by adjustment of the vertical amplitude and the bottom by adjustment of the vertical slope. After the vertical picture alignment the picture is positioned in the horizontal direction by adjustment of the EW width and the horizontal shift. Finally (if necessary) the left- and right-hand sides of the picture are aligned in parallel by adjusting the EW trapezium control.

To obtain the full range of the vertical zoom function the adjustment of the vertical geometry should be carried out at a nominal setting of the zoom DAC at position 19 HEX.

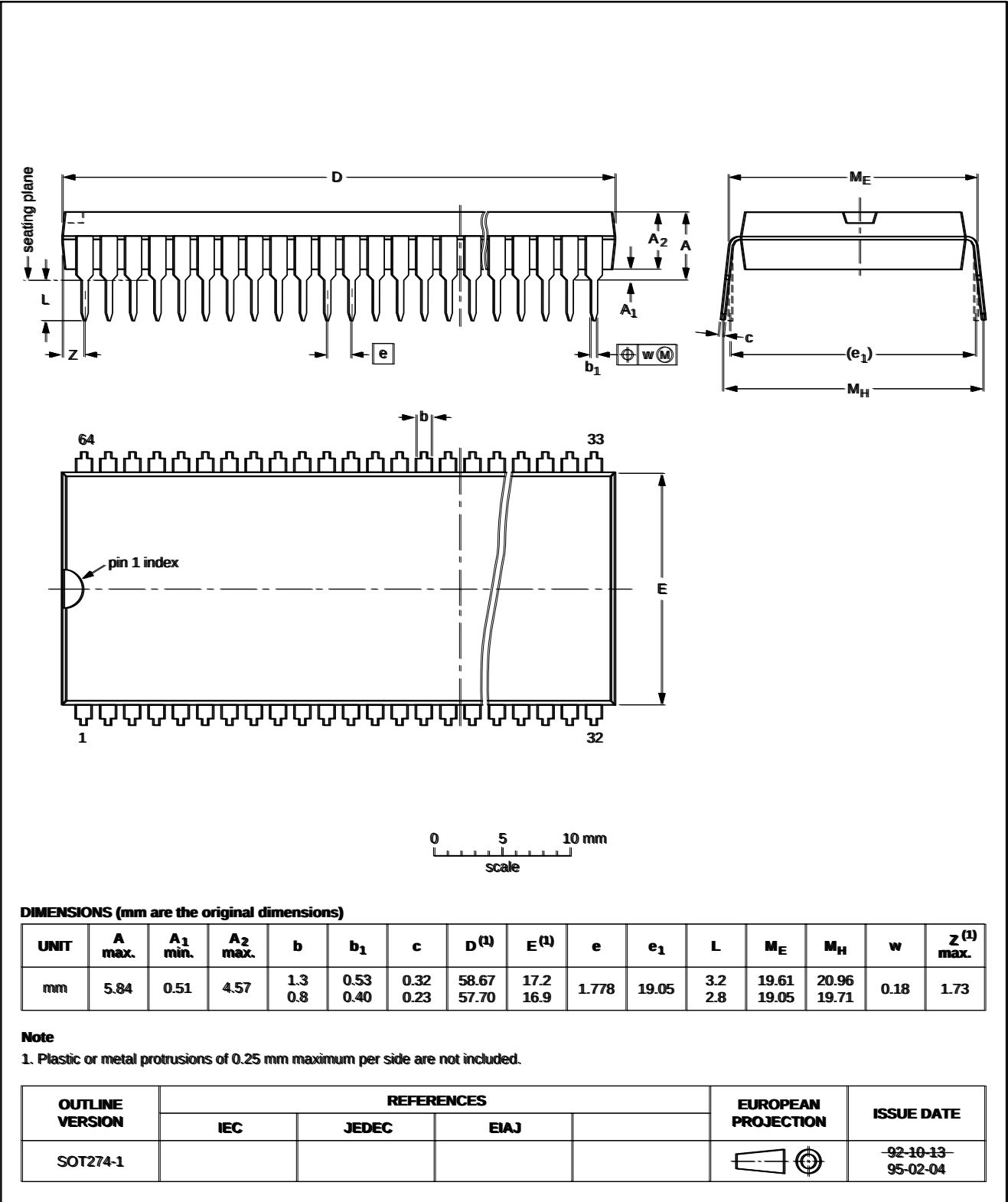
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PACKAGE OUTLINE

SDIP64: plastic shrink dual in-line package; 64 leads (750 mil)

SOT274-1



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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC package Databook"* (order code 9398 652 90011).

SDIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

QFP

REFLOW SOLDERING

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For details, refer to the Drypack information in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

WAVE SOLDERING

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

TV signal processor-Teletext decoder with embedded μ -Controller

TDA935X/6X/8X series

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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